

# Bolt Schematic

## Whiskey Lake

2018/12/13

REV : A00

*DY : None Installed*

*UMA: UMA only installed*

*OPS: DISCRTE OPTIMUS installed*

*TypeC: CCG4*

*TypeC\_5V\_OUT: provide external device power 5V*

*TypeC\_PWR\_IN: Provide system power via typeC connector.*

*8111H:Reltek LAN RTL811H*

*81106E:Reltek LAN RTL8106E*

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size

A3

Document Number

**BOLT WHL**

Rev

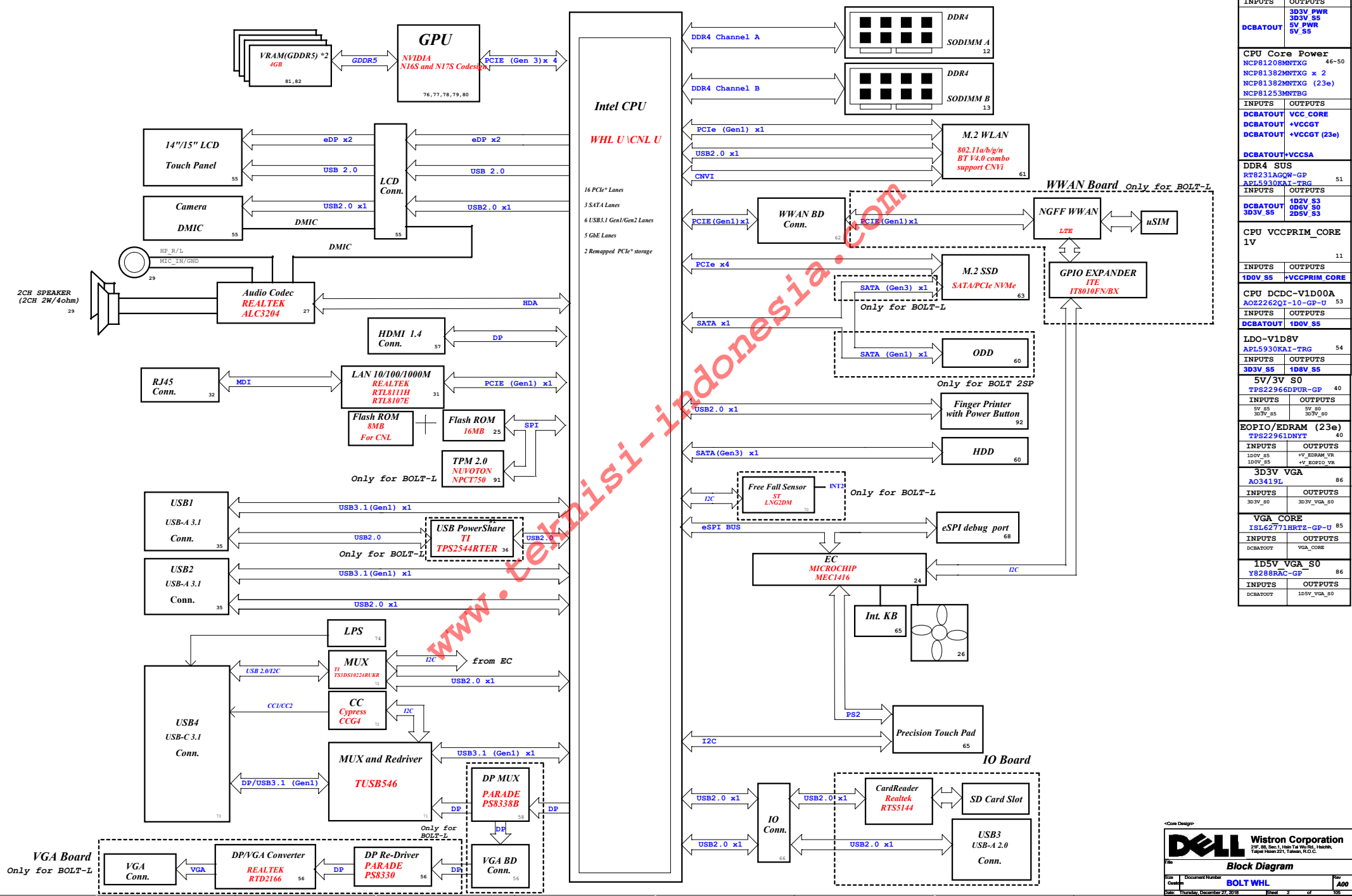
**A00**

Date: Thursday, December 27, 2018

Sheet 1 of 105

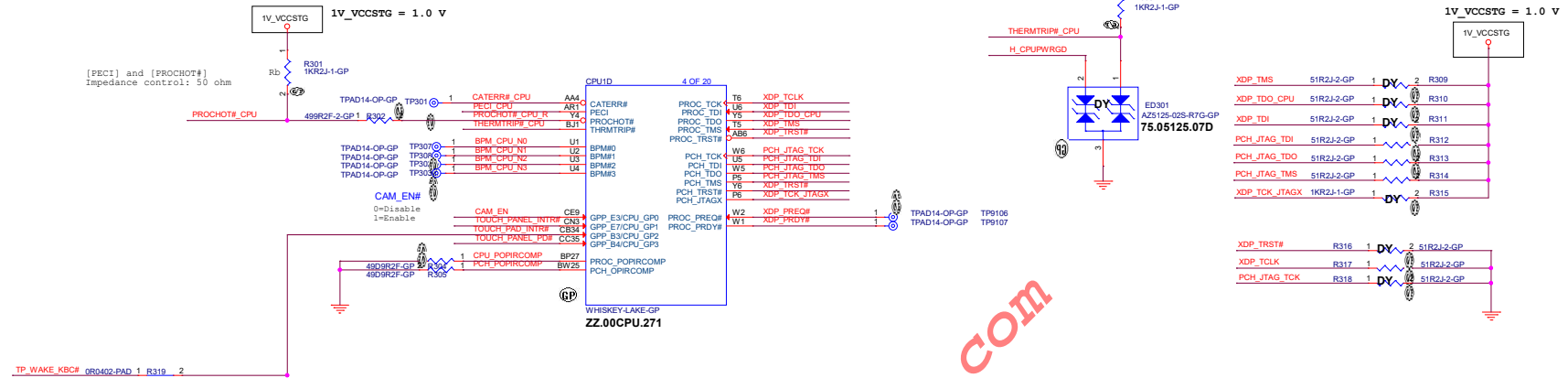
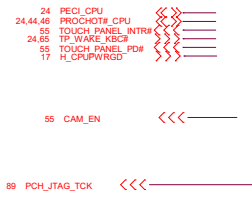
Project Code : 4PD0G7010001  
PCB P/N : 18763  
Revision : SD

# Bolt WHL Block Diagram

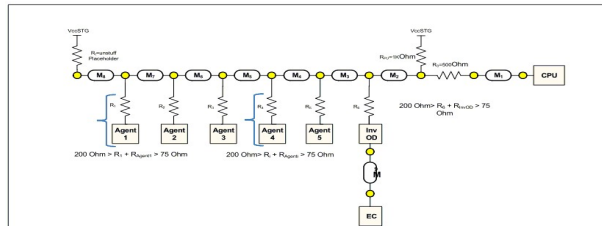


CHARGER	
ISL88739	44
INPUTS	
AD+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	
DCBATOUT	303V_PWR 303V_SS 5V_PWR 5V_SS
CPU Core Power	
NCP81208MNTXG	46~50
NCP81382MNTXG x 2	
NCP81382MNTXG (23e)	
NCP81253MNTBG	
INPUTS	
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT+VCCSA	
DDR4 SUS	
RT8231AGW-GP	51
APL5930KAI-TRG	
INPUTS	
DCBATOUT	102V_S3 303V_S3 205V_S3
CPU VCCPRIM_CORE	
1V	11
INPUTS	
100V_SS	+VCCPRIM_CORE
CPU DCDC-V1D00A	
AO22262QI-10-GP-U	53
INPUTS	
DCBATOUT	100V_SS
LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	
303V_SS	108V_SS
5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	
5V_SS 303V_SS	5V_S0 303V_S0
EOP10/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	
100V_SS 100V_SS	+V_EDRAM_VR +V_EOP10_VR
3D3V VGA	
AO3419L	86
INPUTS	
303V_SS	303V_VGA_S0
VGA CORE	
ISL6271HRTZ-GP-U	85
INPUTS	
DCBATOUT	VGA_CORE
1D5V VGA S0	
Y8288RAC-GP	86
INPUTS	
DCBATOUT	1D5V_VGA_S0

**Main FUNC = CPU**



(#575412) PROCHOT# Routing Guidelines

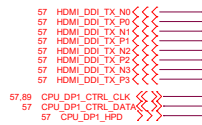


**Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)**

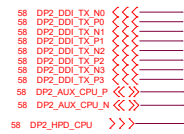
Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1495.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254		10000	
<b>Topology Guidelines</b>							
Platform resistors values			Rpu=1KΩ, Rs=500Ω, Ri+Ragen=75-200Ω, R6+Rinvod=75-200Ω				
Platform resistors tolerances			± 5%				

# Main FUNC = CPU

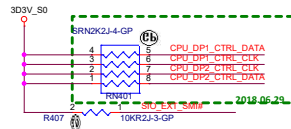
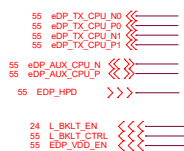
## HDMI 1.4B



## TO DP MUX



## EDP



5.2.7 Compensation Signal Routing Guidelines

Signal	Trace	Termination	Resistor Value	Max Length
407_02000	1.0cm	50ohm	330.0 kΩ	100mm

5.2.8 eDP\* Disabling and Termination Guidelines

Signal	Trace	Termination	Resistor Value	Max Length
407_02000	1.0cm	50ohm	330.0 kΩ	100mm

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

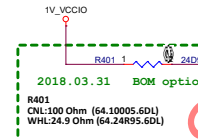
Table 9-1. Pin Straps (Sheet 3 of 4)

#566439

Signal	Usage	When Sampled	Comment
SPI0_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2SD_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPB_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. There should NOT be any on-board device driving it to opposite direction during strap sampling. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz (PLL3) is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RST_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNV1 enable. 1 = Integrated CNV1 disable.

## HDMI 1.4B

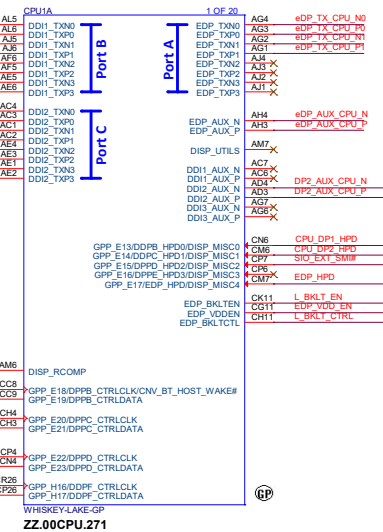
## TO DP MUX



Pin Straps (Sheet 4 of 4)

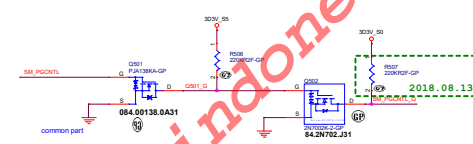
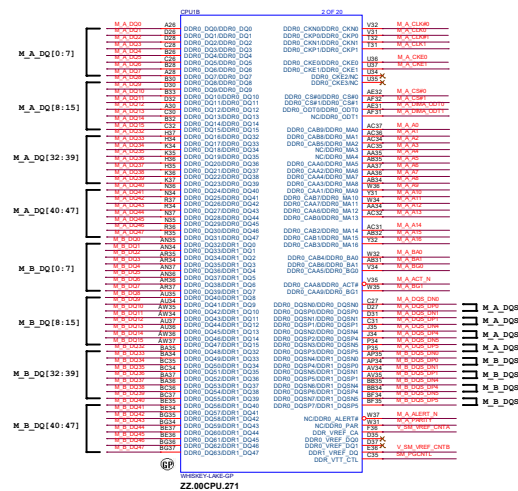
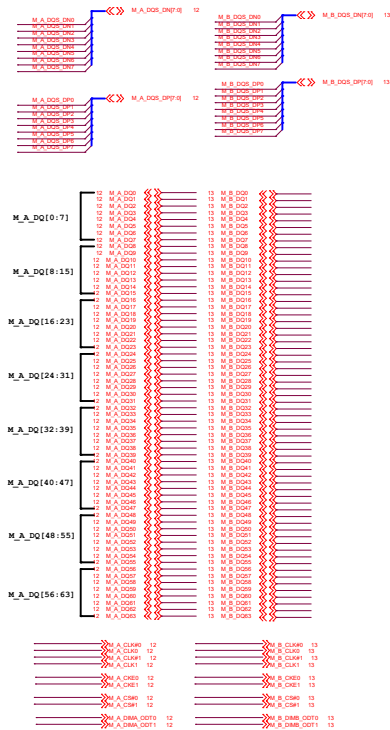
#566439

Signal	Usage	When Sampled	Comment
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% <b>Note:</b> This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. <b>Warning:</b> This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

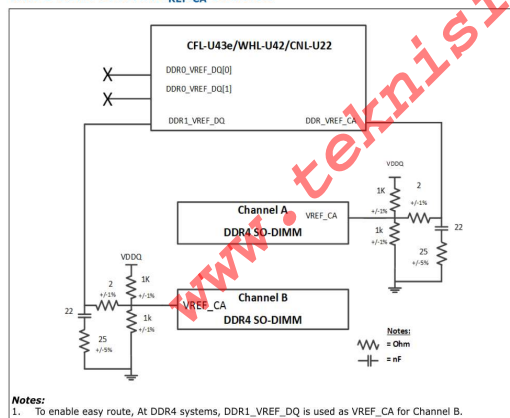




DDR4 ball type: Non-Interleaved Type



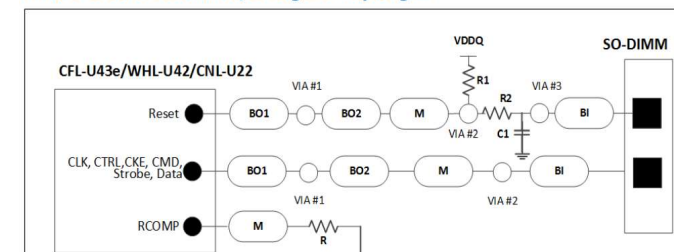
**Figure 4-1. WHL U DDR4 SODIMM V<sub>REF-CA</sub> Overview**



**Notes:**

1. To enable easy route, At DDR4 systems, DDR1\_VREF\_DQ is used as VREF\_CA for Channel B.

## WHL U DDR4 SODIMM T3/8L Signals Topologies



**Note:** DRAM\_RST C1 capacitor should not be installed

RCOMP (0/1/2)	M	US/SL	500			15	20	25	CFL-U436/ WHL-U42; 121/80.6/ 100  CNI-U22; 100/100/ 100
Reset	BO1	US	500	8000		3		6	R1=470 [5%] R2=0
	BO2	SL	800-BO1			3.5		12	
	M	SL			50	4		20	C1=0.1uF (no stuff)
	BI	US				4		20	

DOI: 10.3390/000000000000



Main FUNC = CPU

15 CFG3 <<>>  
15 CFG4 <<>>

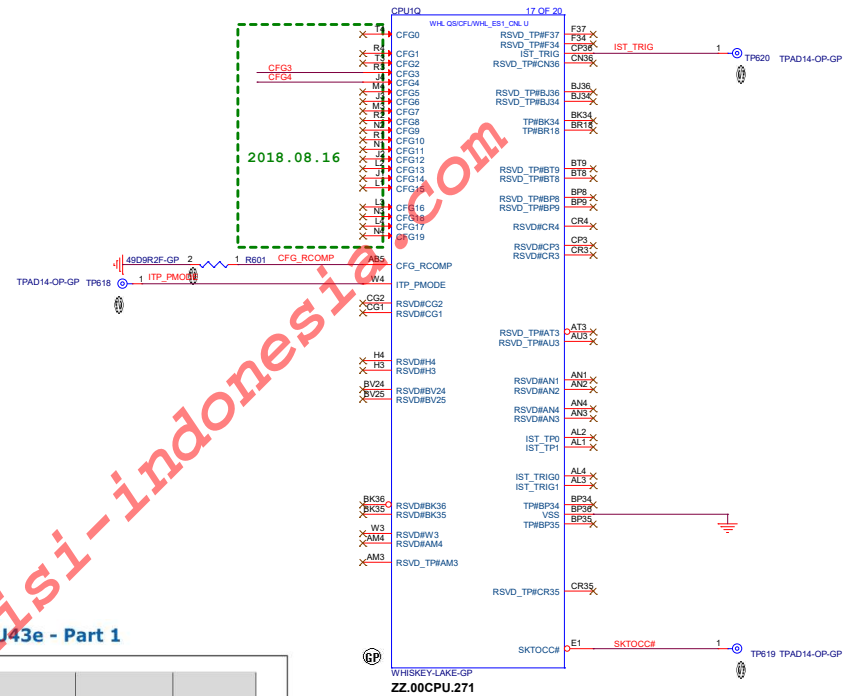
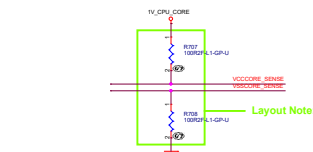
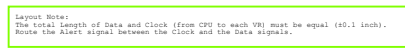


Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIE_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 162Ω ±1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCie					X	
USB2						X

BOLT 15 32bit 0822



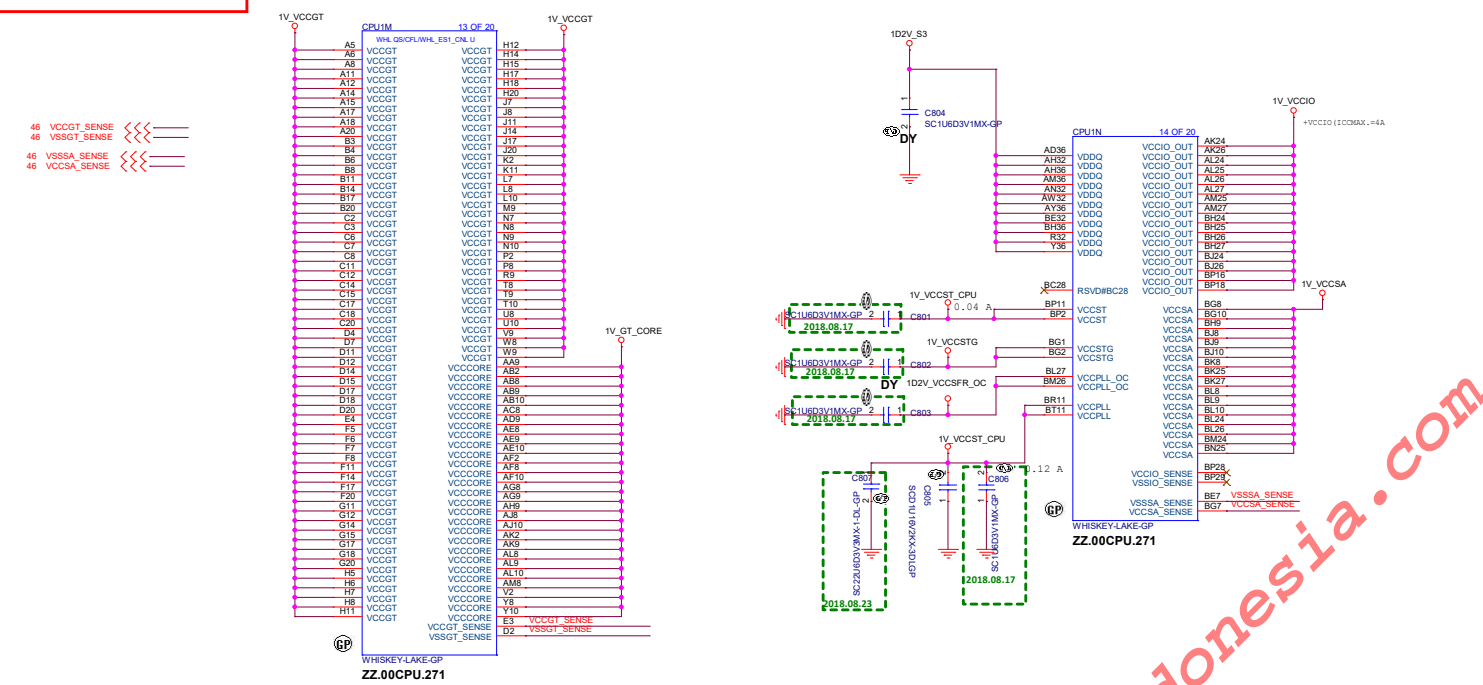
VIDSOUT, VIDSCK, VIDSALERT#	
VIDS Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Q, Rpu2=100Q, Rs1=0Q, Rs2=10Q
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Q, Rs1=0Q, Rs2=49.9Q
VIDSALERT# platform resistors	Rpu1=56Q, Rpu2=Empty, Rs1=220Q, Rs2=0Q
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

The diagram illustrates a 100 ohm catch resistor circuit for an IMVP8/9 Controller. The controller is connected to a Vss\_SENSE pin, which is connected to a Vss Plane. A 100 ohm catch resistor (R1-R2) is connected between the Vss Plane and the Vss\_SENSE pin. The diagram also shows the Processor Package and Socket, with a Die connected to the Vss Plane. The resistor is labeled #575412.

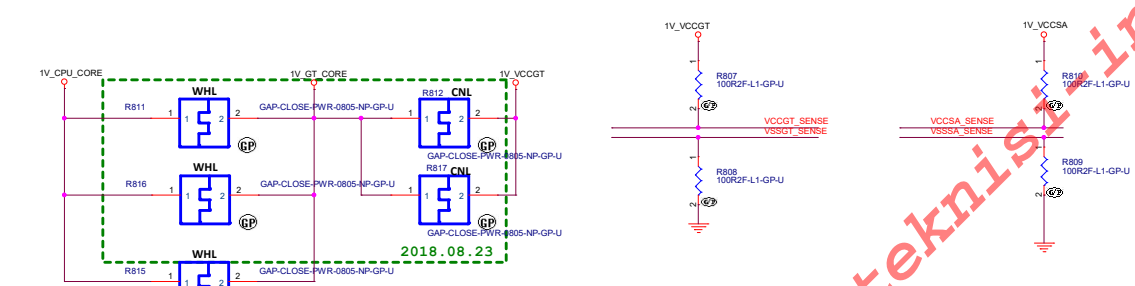
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	50Ω	<25 mils
VCC <sub>GT</sub> _SENSE / VSS <sub>GT</sub> _SENSE			
VCC <sub>SA</sub> _SENSE / VSS <sub>SA</sub> _SENSE		NA	
VCC <sub>IO</sub> _SENSE / VSS <sub>IO</sub> _SENSE <sup>[1]</sup>			

- R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc\_SENSE/Vss\_SENSE line resistance.

Main FUNC = CPU



Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



Design Target	CPU support	Stiffing options for compatibility	Incremental VR BOM vs KBL	Incremental board area vs. KBL
Cost optimized entry design (C13 SMBO-ICP)	CNL only	None	No increase expected for CNL vs. KBL U22	~0mm² vs. KBL U22
Premium design (C17-C13)	WHL only	None	Load line change anticipated to drive incremental cost vs. KBL R	TBD
Scalable mainstream design (C17-ICP)	WHL and CNL	Jumpers vary by SKU: 3 if WHL 1 if CNL	Load line change on WHL anticipated to drive incremental cost vs. KBL R No increase expected for CNL vs. KBL U22	TBD

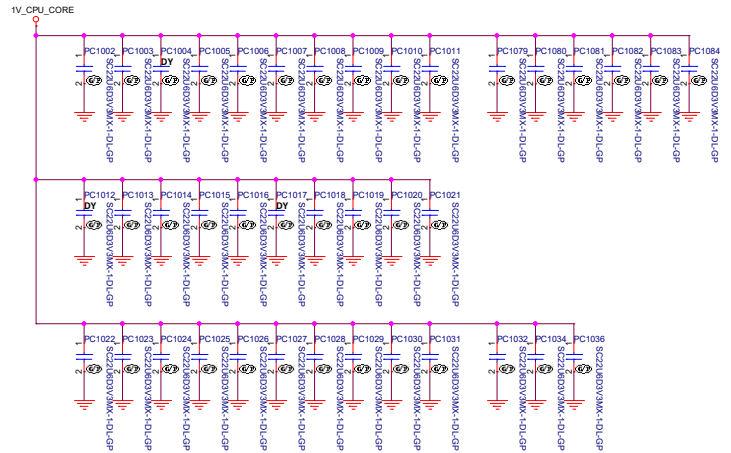
Main Func = CPU

(Blanking)

www.teknisi-indonesia.com

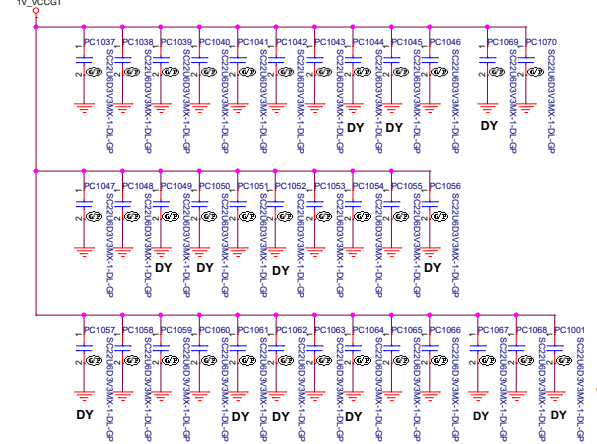
# 1V\_CPU\_CORE

22U 0603 x 39 (3DY)



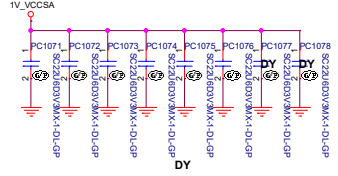
# VCCGT

22U 0603 x 35 (3 DY)



# VCCSA

22U 0603 x 8 (3DY)



## KBL-R U42 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR) 1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VDDQ Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCPLL Power Plane at V1P0A VR output	1x 0.1uF 0402	Placed at primary side near to VR output

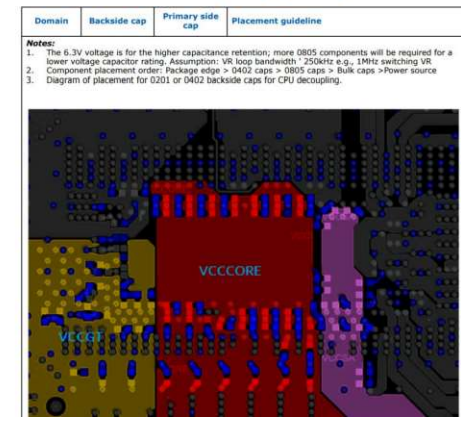
**Notes:**

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

## KBL-R U42 Decoupling Requirements (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
VCCGT	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
VCCSA	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
VCCIO		4x 1 uF 0402	Place as close to the package as possible
VDDQ		4x 10 uF 0402	Place as close to the package as possible
VDDQ		3 x 22 uF 0603	Place as close to the package as possible
VDDQ		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQ BGA routing should not exceed 48mm (RdC). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
VCCPLL		1x 1 uF 0402	Place as close to the package as possible.
VCCPLL_DC		1x 1 uF 0201	Do not route VCCPLL, VCCPLL_DC, VCCGT closest adjacent layer over any power net other than ground.
VCCGT		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

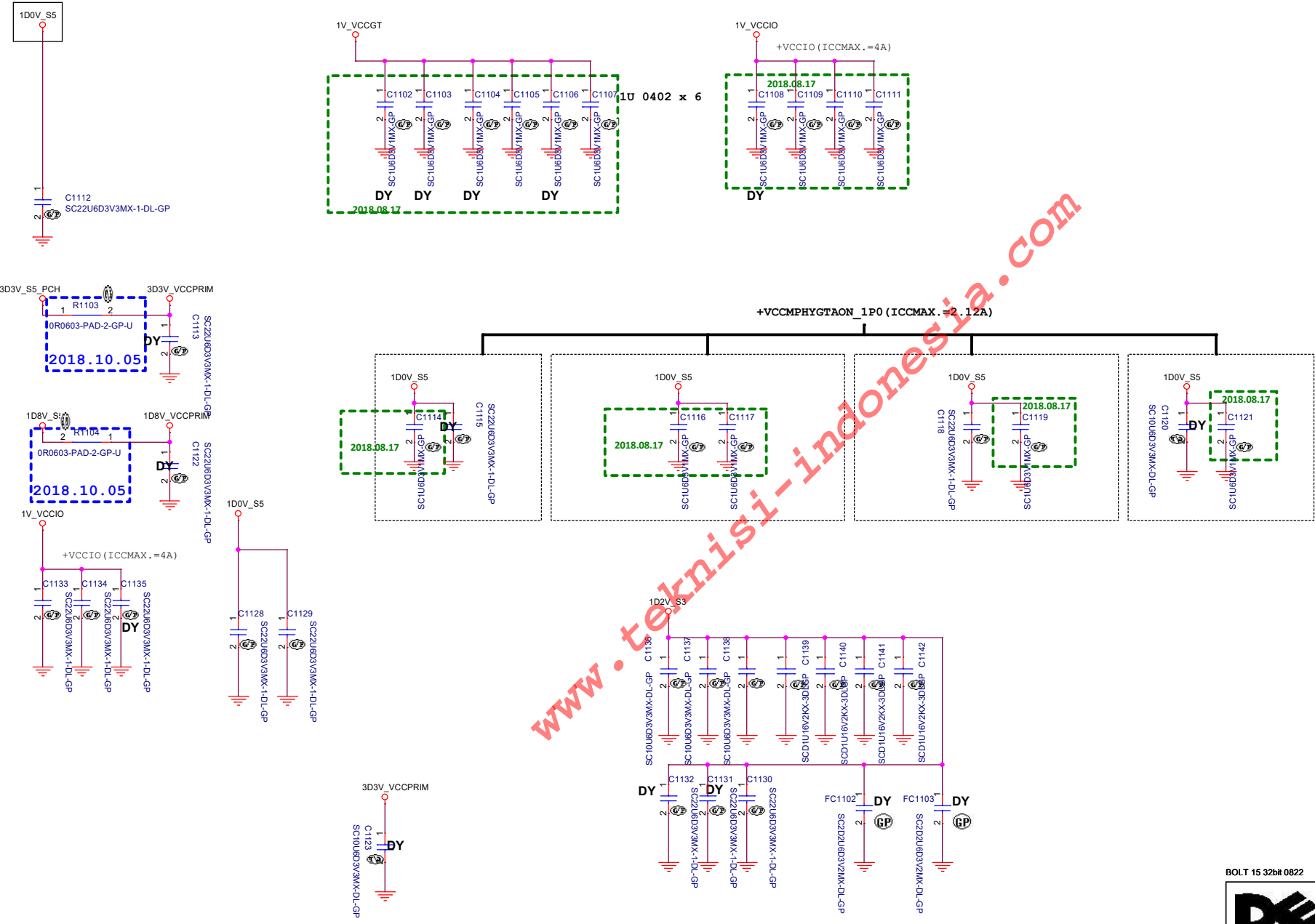
## KBL-R U42 Decoupling Requirements (Sheet 2 of 2)



<Core Design>



PCH DERIVED RAILS UNSLICED GT VCCIO



**Layout Note:**

1uF:  
C1174 near N15  
C1180 near K15  
C1173 near AF20  
C1172 near N18  
C1175 near AB19  
22uF :  
C1182 C1184 near N15  
10uF:  
C1176 near N15

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU\_(Power CAP2)

Size

A3

Document Number

RogueOne 13"

Rev

A00

Date:

Thursday, December 27, 2018

Sheet

11

of

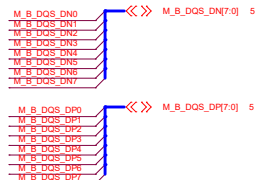
106

www.teknisi-indonesia.com






Main Func  
= MEMORY



(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)_SODIMM _SODIMM4</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 14	of 106

13.07. 0000 <<<<<  
 13.08. 0000 <<<<<  
 13.09. 0000 <<<<<  
 13.10. 0000 <<<<<  
 13.11. 0000 <<<<<  
 13.12. 0000 <<<<<  
 13.13. 0000 <<<<<  
 13.14. 0000 <<<<<  
 13.15. 0000 <<<<<  
 13.16. 0000 <<<<<  
 13.17. 0000 <<<<<  
 13.18. 0000 <<<<<  
 13.19. 0000 <<<<<  
 13.20. 0000 <<<<<  
 13.21. 0000 <<<<<  
 13.22. 0000 <<<<<  
 13.23. 0000 <<<<<  
 13.24. 0000 <<<<<  
 13.25. 0000 <<<<<  
 13.26. 0000 <<<<<  
 13.27. 0000 <<<<<  
 13.28. 0000 <<<<<  
 13.29. 0000 <<<<<  
 13.30. 0000 <<<<<  
 13.31. 0000 <<<<<  
 13.32. 0000 <<<<<  
 13.33. 0000 <<<<<  
 13.34. 0000 <<<<<  
 13.35. 0000 <<<<<  
 13.36. 0000 <<<<<  
 13.37. 0000 <<<<<  
 13.38. 0000 <<<<<  
 13.39. 0000 <<<<<  
 13.40. 0000 <<<<<  
 13.41. 0000 <<<<<  
 13.42. 0000 <<<<<  
 13.43. 0000 <<<<<  
 13.44. 0000 <<<<<  
 13.45. 0000 <<<<<  
 13.46. 0000 <<<<<  
 13.47. 0000 <<<<<  
 13.48. 0000 <<<<<  
 13.49. 0000 <<<<<  
 13.50. 0000 <<<<<  
 13.51. 0000 <<<<<  
 13.52. 0000 <<<<<  
 13.53. 0000 <<<<<  
 13.54. 0000 <<<<<  
 13.55. 0000 <<<<<  
 13.56. 0000 <<<<<  
 13.57. 0000 <<<<<  
 13.58. 0000 <<<<<  
 13.59. 0000 <<<<<  
 13.60. 0000 <<<<<  
 13.61. 0000 <<<<<  
 13.62. 0000 <<<<<  
 13.63. 0000 <<<<<  
 13.64. 0000 <<<<<  
 13.65. 0000 <<<<<  
 13.66. 0000 <<<<<  
 13.67. 0000 <<<<<  
 13.68. 0000 <<<<<  
 13.69. 0000 <<<<<  
 13.70. 0000 <<<<<  
 13.71. 0000 <<<<<  
 13.72. 0000 <<<<<  
 13.73. 0000 <<<<<  
 13.74. 0000 <<<<<  
 13.75. 0000 <<<<<  
 13.76. 0000 <<<<<  
 13.77. 0000 <<<<<  
 13.78. 0000 <<<<<  
 13.79. 0000 <<<<<  
 13.80. 0000 <<<<<  
 13.81. 0000 <<<<<  
 13.82. 0000 <<<<<  
 13.83. 0000 <<<<<  
 13.84. 0000 <<<<<  
 13.85. 0000 <<<<<  
 13.86. 0000 <<<<<  
 13.87. 0000 <<<<<  
 13.88. 0000 <<<<<  
 13.89. 0000 <<<<<  
 13.90. 0000 <<<<<  
 13.91. 0000 <<<<<  
 13.92. 0000 <<<<<  
 13.93. 0000 <<<<<  
 13.94. 0000 <<<<<  
 13.95. 0000 <<<<<  
 13.96. 0000 <<<<<  
 13.97. 0000 <<<<<  
 13.98. 0000 <<<<<  
 13.99. 0000 <<<<<  
 14.00. 0000 <<<<<

GPP_B18 / GSP10_MOSI	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode. (Default)</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PCH_PWROK is high.</li> <li>This signal is in the primary well.</li> </ol>
----------------------	-----------	--------------------------	--

GPP\_B18



GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
--------------------	---------------------	------------------------	--

GPP\_C2



GPP_C5 / SMLDAlert#	eSPI or LPC	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>LPC</b> is selected (for EC). (Default)</p> <p>1 = <b>eSPI</b> is selected (for EC).</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol> <p><b>Warning:</b> If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' (SAFS is disabled).</p>
---------------------	-------------	------------------------	---

GPP\_C5



SP10_MOSI	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
-----------	----------	------------------------	---

SP10\_MOSI



GPP_D12 / ISH_SPI_MOSI / GSP12_MOSI	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
-------------------------------------	----------	------------------------	---

GPP\_D12



SP10_I02	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
----------	----------	------------------------	---

SP10\_I02



SP10_I03	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
----------	----------	------------------------	---

SP10\_I03



HDA_SDO / I2SD0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Enable</b> security measures defined in the Flash Descriptor. (Default)</p> <p>1 = <b>Disable</b> Flash Descriptor Security (guarded). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PCH_PWROK is high.</li> <li>This signal is in the primary well.</li> </ol>
---------------------	------------------------------------	--------------------------	---

HDA\_SDO



GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.</p> <p>0 = 38.4 MHz XTAL frequency selected. (Default)</p> <p>1 = 24MHz XTAL frequency selected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
---------	-----------------------	------------------------	---

GPP\_H21



GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	<p>An external pull-up or pull-down is required.</p> <p>0 = Integrated CNV enable.</p> <p>1 = Integrated CNV disable.</p>
---------------------	---------------------	------------------------	---

GPP\_F6



INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	<p>External pull-up or pull-down is required</p> <p>0 = 3.3V supply is 3.3V +/- 5%</p> <p>1 = 3.3V supply is 3.0V +/- 5%</p> <p><b>Note:</b> This strap should only be used for specific targeted 1S battery systems.</p>
------------	-------------	--	---

INPUT3VSEL



GPD7	Reserved	Rising edge of DSIW_PWROK	<p>External pull-up is required. Recommend 100K.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
------	----------	---------------------------	--

GPD7



GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Master Attached Flash Sharing (MAFS) enabled (Default)</p> <p>1 = Slave Attached Flash Sharing (SAFS) enabled.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol> <p><b>Warning:</b> This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC Strap is configured to '0' (eSPI is disabled).</p>
---------	-------------------------	------------------------	---

GPP\_H23



NAME	ONLY/PROCESSOR/BIOS/ENABLED	ONLY/PROCESSOR/BIOS/ENABLED
ONLY/PROCESSOR/BIOS/ENABLED	ONLY/PROCESSOR/BIOS/ENABLED	ONLY/PROCESSOR/BIOS/ENABLED

PCH strap pin:

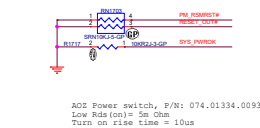
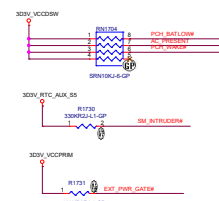
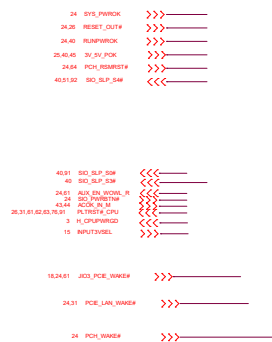


NAME	ONLY/PROCESSOR/BIOS/ENABLED	ONLY/PROCESSOR/BIOS/ENABLED
ONLY/PROCESSOR/BIOS/ENABLED	ONLY/PROCESSOR/BIOS/ENABLED	ONLY/PROCESSOR/BIOS/ENABLED

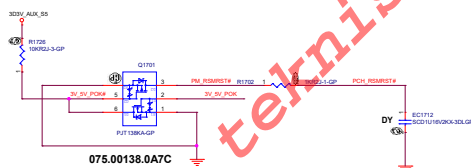
PCH strap pin:



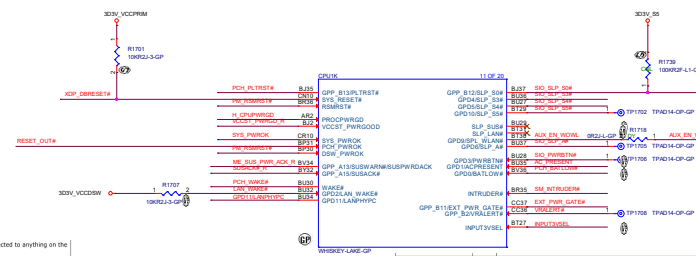




AOS Power switch, P/N: 074.01334.0093  
Low Rds(on) = 5m Ohm  
Turn on rise time = 10us

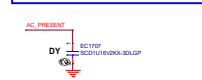


www.teknisi-indonesia.com



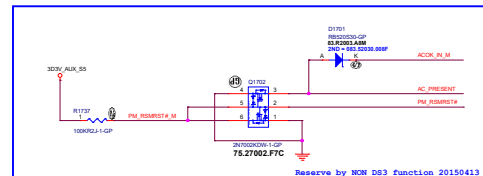
Signal	Usage	When Sampled	Comment
INPUTVSEL	3.0V Select	Input pin must always be driven to a valid logic level	Strapped high if PCH's VCC3SW_3PS rail is 3.0V +/- 5%; else PCH's VCC3SW_3PS rail is 3.3V +/- 5%. This pin is in the VCC3SW_3PS well.

BASEG0#1: Pull-up required when I.E not implemented.



R1722 & R1708 modify to 100k and 0.01uF at DV1

#543016 Rev0.7  
1. VCC3SW\_PWROD is only 1.0 V tolerant.  
2. VCC3SW\_PWROD must go Low during its pwr states, regardless of the voltage level of VCC3SW



Reserve by NON DB3 function 20150413



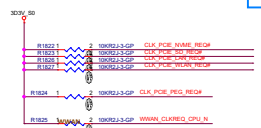
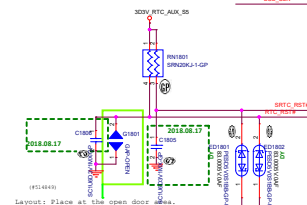
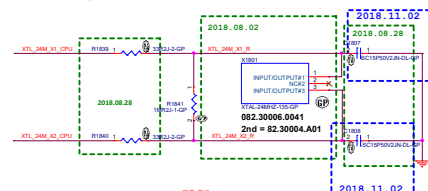
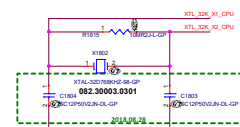
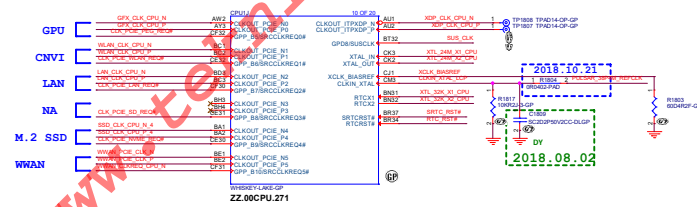
ZZ.00CPU.27

Table 3-1: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash		Table 3-2: Functional Strap Definitions (Sheet 2 of 3)	
ESPI Enable Strap (ESPI_Enable Value (0: LPC; 1: eSPI))	Boot BIOS Strap (BBS) Value (0: LPC; 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC cover eSPI in Peripheral Channel) (refer to Section 3.1.4 for details)

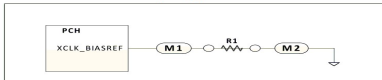
Signal	Strap	When Sampled	Comment
eSPI or LPC	SMD_ALERT# GPP_C6	Rising edge of RSMRST#	This signal has a weak internal pull-down. This field determines the destination of accesses to the eSPI or SPI Flash. The destination is either SPI Flash Destination (BBS, Devices), Function, or EC, (BCN, or EC).
			<div> <div>Bit 6</div> <div>Boot BIOS Destination SPI (Default)</div> <div>1</div> <div>LPC</div> </div> <p><b>Notes:</b></p> <ul style="list-style-type: none"> <li>The internal Pull-down is disabled after RST# or PLEST# in asserts.</li> <li>If option 1 (LPC) is selected, BIOS may still be placed on EC, but all platforms are required to have a SPI Flash connected directly to the PCH or SPI bus with a valid descriptor in order to boot.</li> <li>When the signal is sampled, the internal Pull-down strap is using Boot BIOS Destination but will not reset SPI address, limited by their own integrated GDL LARs.</li> <li>This signal is in the primary use.</li> </ul>
eSPI or LPC	SMD_ALERT# GPP_C3	Rising edge of RSMRST#	This signal has a weak internal Pull-down. If eSPI is selected for EC, (Default) If eSPI is selected for EC.
			<p><b>Notes:</b></p> <ul style="list-style-type: none"> <li>The internal Pull-down is disabled after RSMRST#</li> <li>This signal is in the primary use.</li> </ul>



CLKIN_XTAL	I	<b>XTAL Clock Input:</b> Single ended integrated CNV (Connectivity) XTAL clock input
------------	---	--

Group	Signal Name	Description
System Management	INTRUDER#	Intruder Detect: This signal can be set to disable system if box detected open.
RTC	SRTCRST#	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed.
RTC	RTCRST#	RTC Reset: When asserted, this signal resets register bits in the RTC well.

Figure 7-11. XCLK Bias Reference Topology

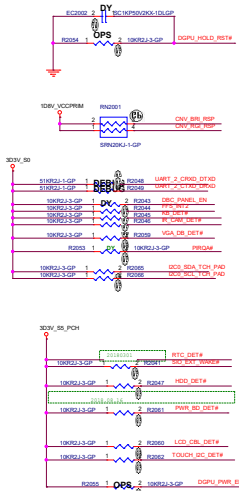
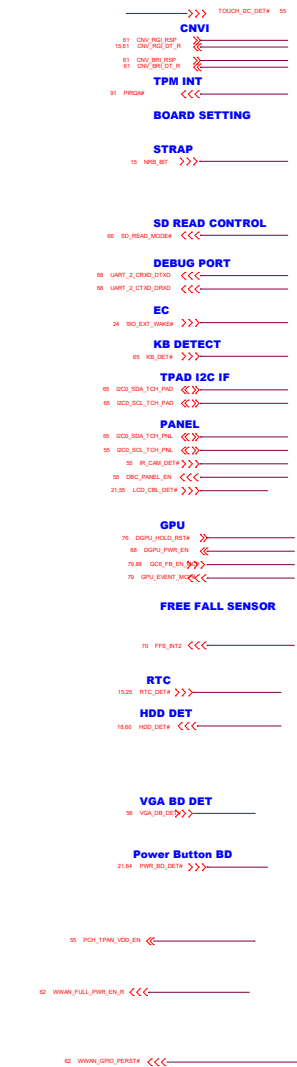


**Table 7-8. XCLK Bias Reference Routing Guideline (Sheet 1 of 2)**

Parameter	Segment	Stack-up	Rule
Reference Plane	M1, M2	MS/SL/DSL	Ground
Single Ended Trace Impedance	M1, M2	MS/SL/DSL	Refer Note
Max Total Length	M1+M2	MS/SL/DSL	1000mil<(25.4mm)
Resistor (R1)			60 Ohm ± 1.0%
Max Transition Via Count			2







2018.08.02

CR14  
PWR\_BD\_DET#  
BLUETOOTH\_EN  
LCD\_CBL\_DET#  
TO\_DB\_DET#  
CNV\_MFUART2\_RXD  
CNV\_MFUART2\_TXD  
WWAN\_BB\_RST#  
1.8V only

CR14  
GPP\_C8/UART0\_RXD  
GPP\_C9/UART0\_TXD  
GPP\_C10/UART0\_RTS#  
GPP\_C11/UART0\_CTS#  
GPP\_F8/CNV\_MFUART2\_RXD  
GPP\_F9/CNV\_MFUART2\_TXD  
GPP\_F23/A4WP\_PRESENT

CR16  
GPP\_F20/EMMC\_RCLK  
GPP\_F21/EMMC\_CLK  
GPP\_F11/EMMC\_CMD  
GPP\_F22/EMMC\_RESET#

CM18  
CM16  
CP18  
CR16  
CN16  
CK15

EMMC\_RCOMP

WHISKEY-LAKE-GP

ZZ.00CPU.271

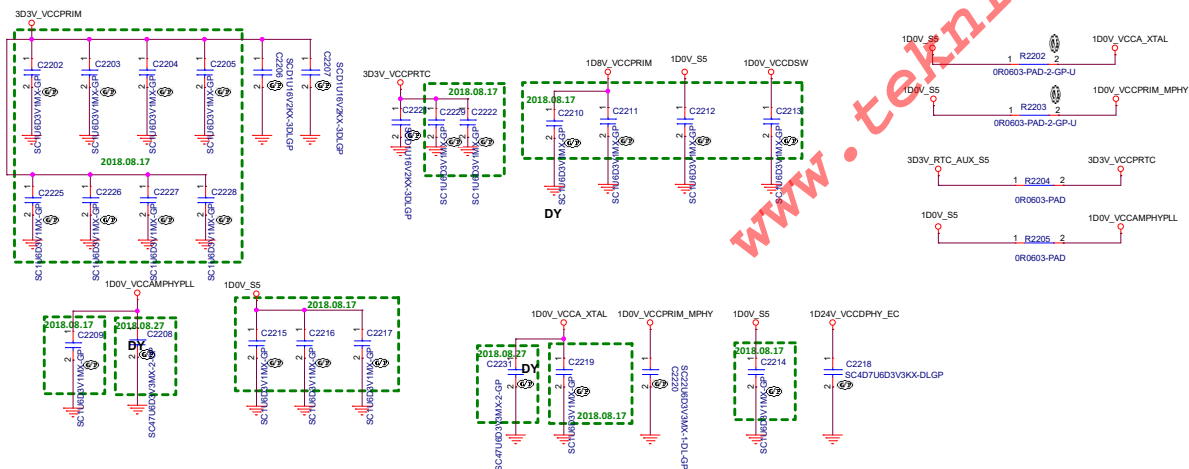
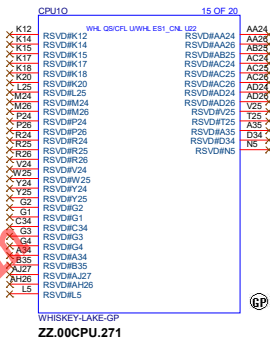
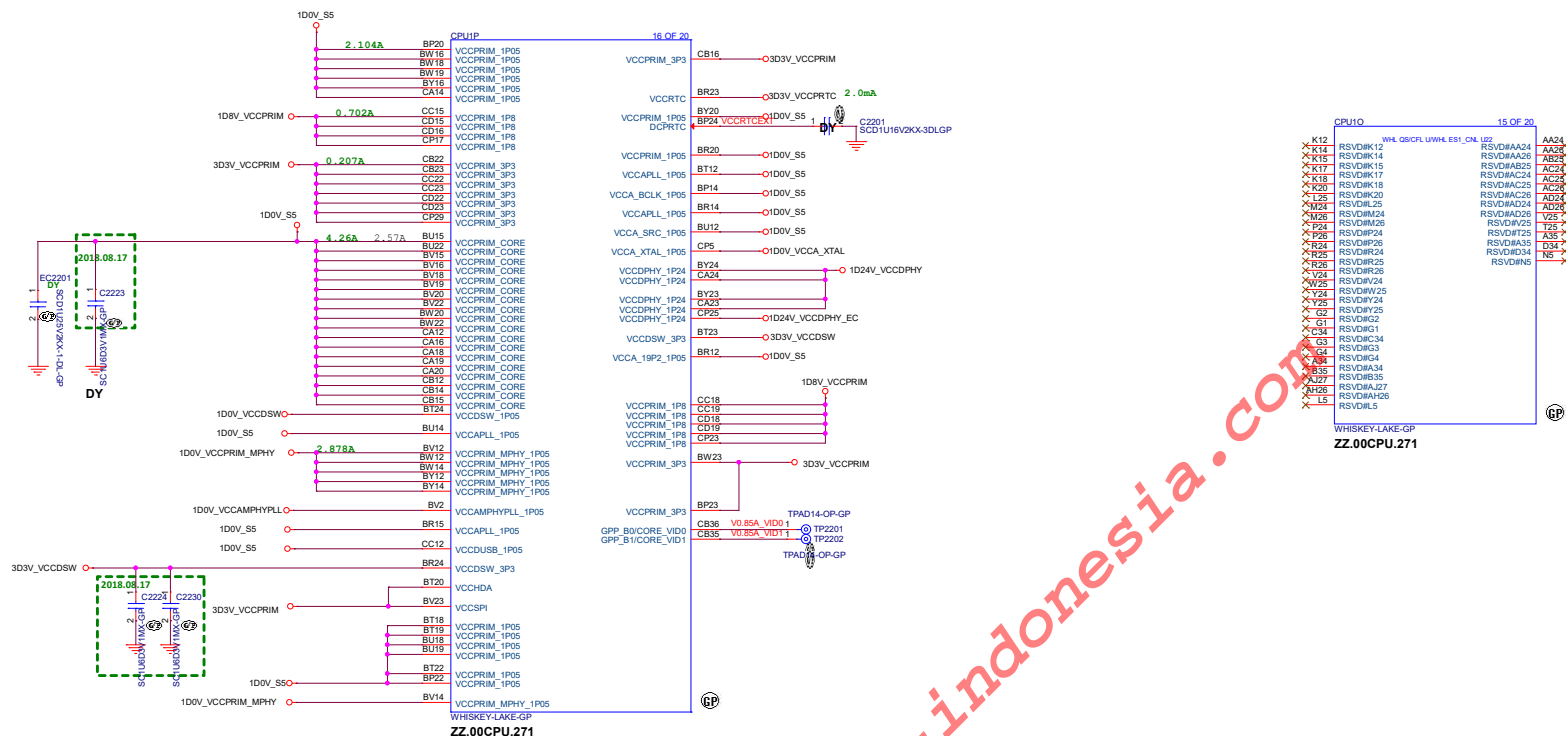
connected standby platform

CLKREQ#	SB_RESET#	Notes
L0 : L	H	
L1.2 : H		
H	H	
H	H	
-	L	Power is removed from modem
H	H	
-	L	
-	L	Power is removed from modem

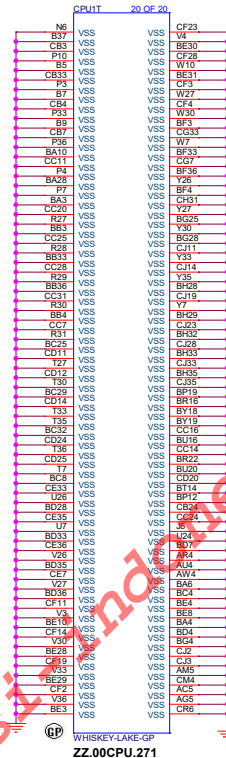
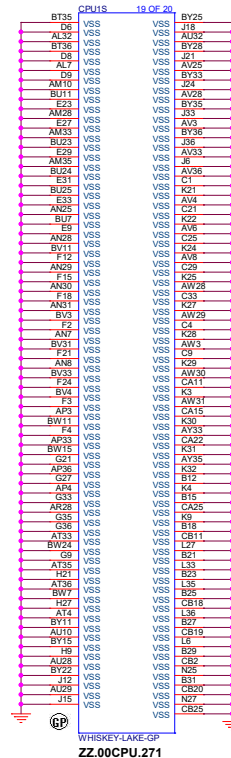
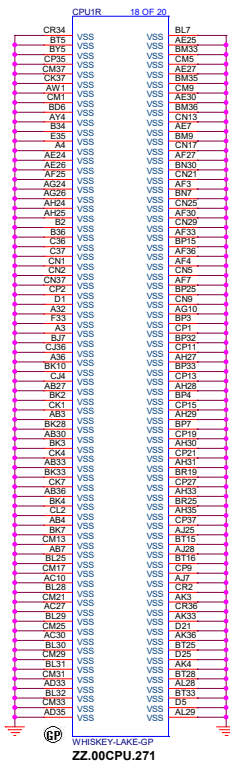
1D8V\_VCCPRIM

1D8V\_VCCPRIM

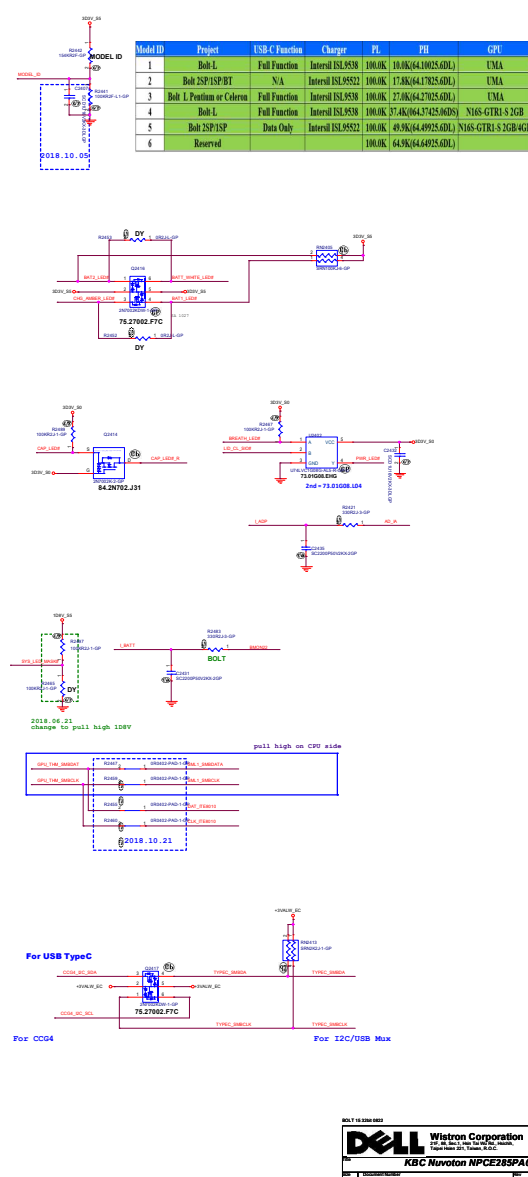
**Main Func = CPU**



**Main Func = CPU**

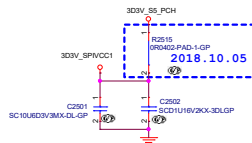


Model ID	Project	USB-C Function	Charger	PL	PH	GPU
1	Bolt-L	Full Function	Interpol ISL9538	100.0K	10.0K/64.19025.GDL	UMA
2	Bolt ZSP1SP-BT	N/A	Interpol ISL9552	100.0K	17.8K/64.17025.GDL	UMA
3	Bolt-L Platform or Colerua	Full Function	Interpol ISL9538	100.0K	27.0K/64.27025.GDL	UMA
4	Bolt-L	Full Function	Interpol ISL9538	100.0K	37.4K/64.37425.GDL	N16- GTRI-5 2GB
5	Bolt ZSP1SP	Data Only	Interpol ISL9552	100.0K	49.9K/64.49925.GDL	N16S- GTRI-5 3GB/G4
6	Reserved			100.0K	64.9K/64.64925.GDL	

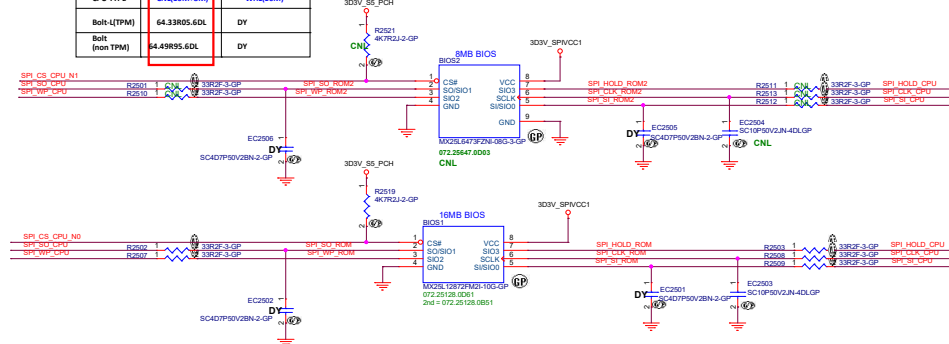


## Main Func = SPI Flash

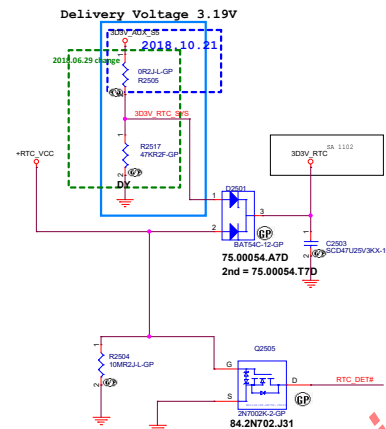
18 SPI\_CS\_CPU\_N1 >>>  
18 SPI\_CS\_CPU\_N0 >>>  
15,18 SPI\_HOLD\_CPU <<<  
24 RTORST\_ON <<<  
53 3V\_SV\_DSW\_OK <<<  
18,91 SPI\_S0\_CPU <<<  
15,18 SPI\_CLK\_CPU <<<  
15,18,91 SPI\_S1\_CPU <<<  
15,20 RTC\_DET# <<<  
24 VCCDSW\_ON <<<  
17,40,45 3V\_SV\_POK <<<



R2502/R2507/R2503/R2508/R2509			
CPU TYPE	CNL(16M+8M)	WHL(16M)	
Bolt-(TPM)	64.33R05.6DL	64.49R95.6DL	
Bolt (non TPM)	064.49R95.56D1	63.R0034.L0L	

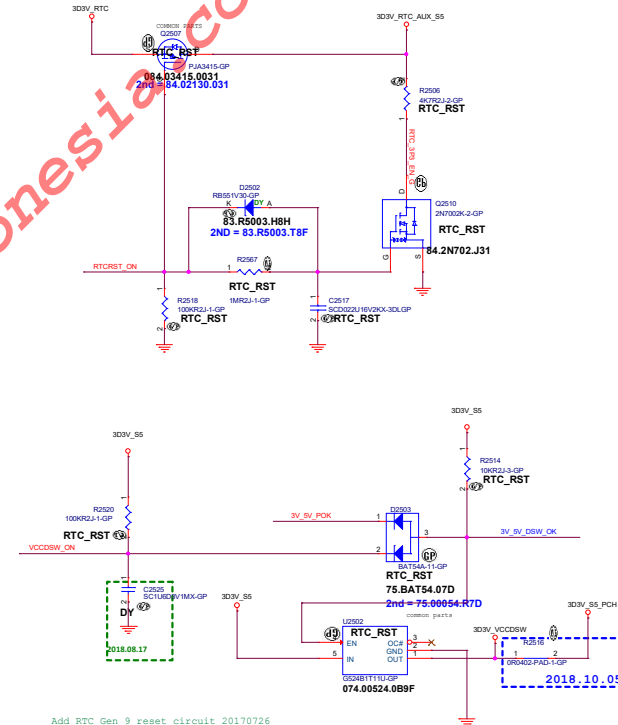


## Main Func = RTC



### 29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



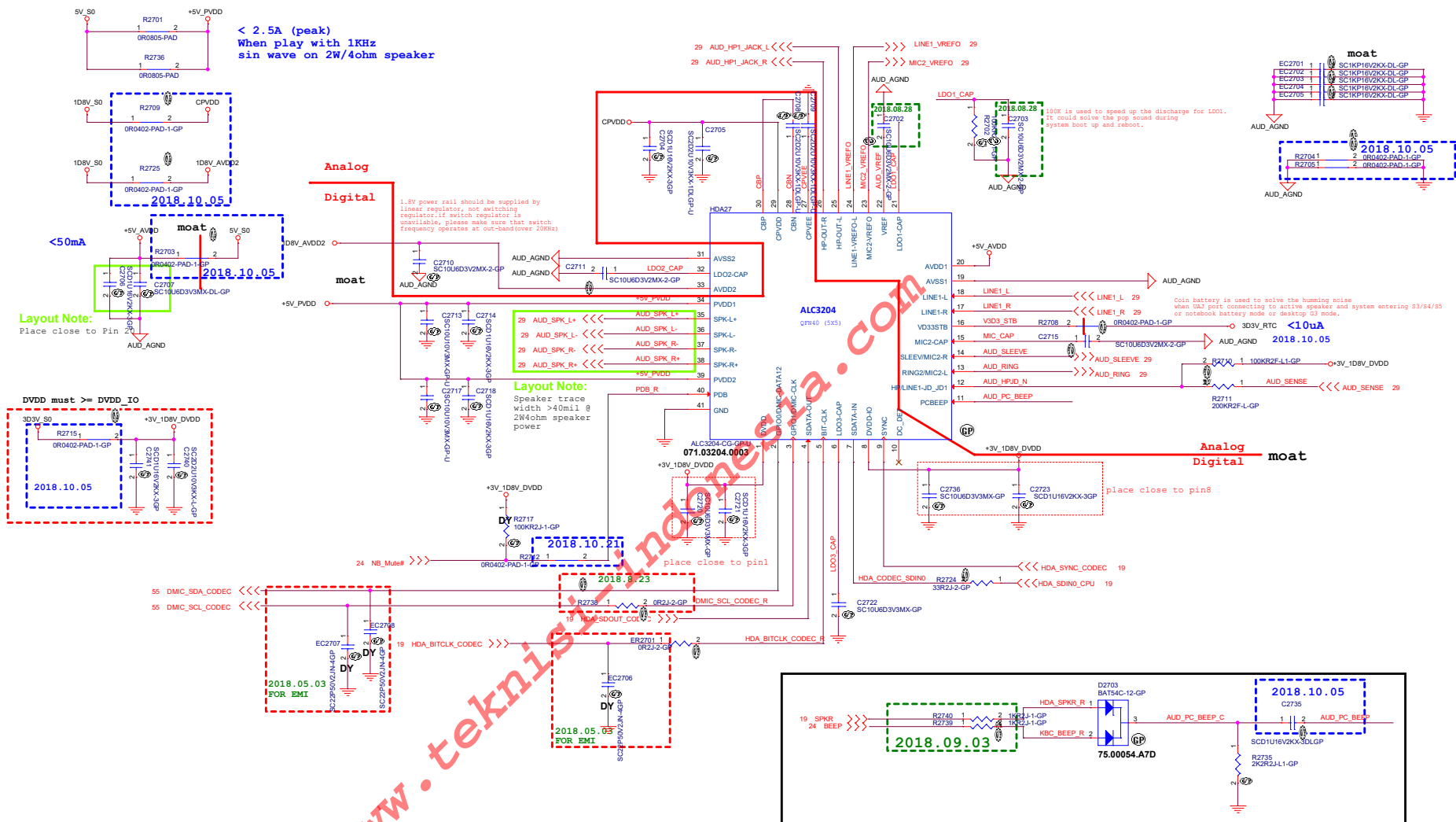
Add RTC Gen 9 reset circuit\_20170726

BOLT 15 32M 0822






**Main Func = Audio**



(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 28	of 105



(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserved)**

Size  
A4

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

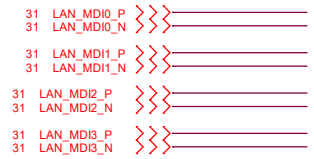
Sheet 30 of 105



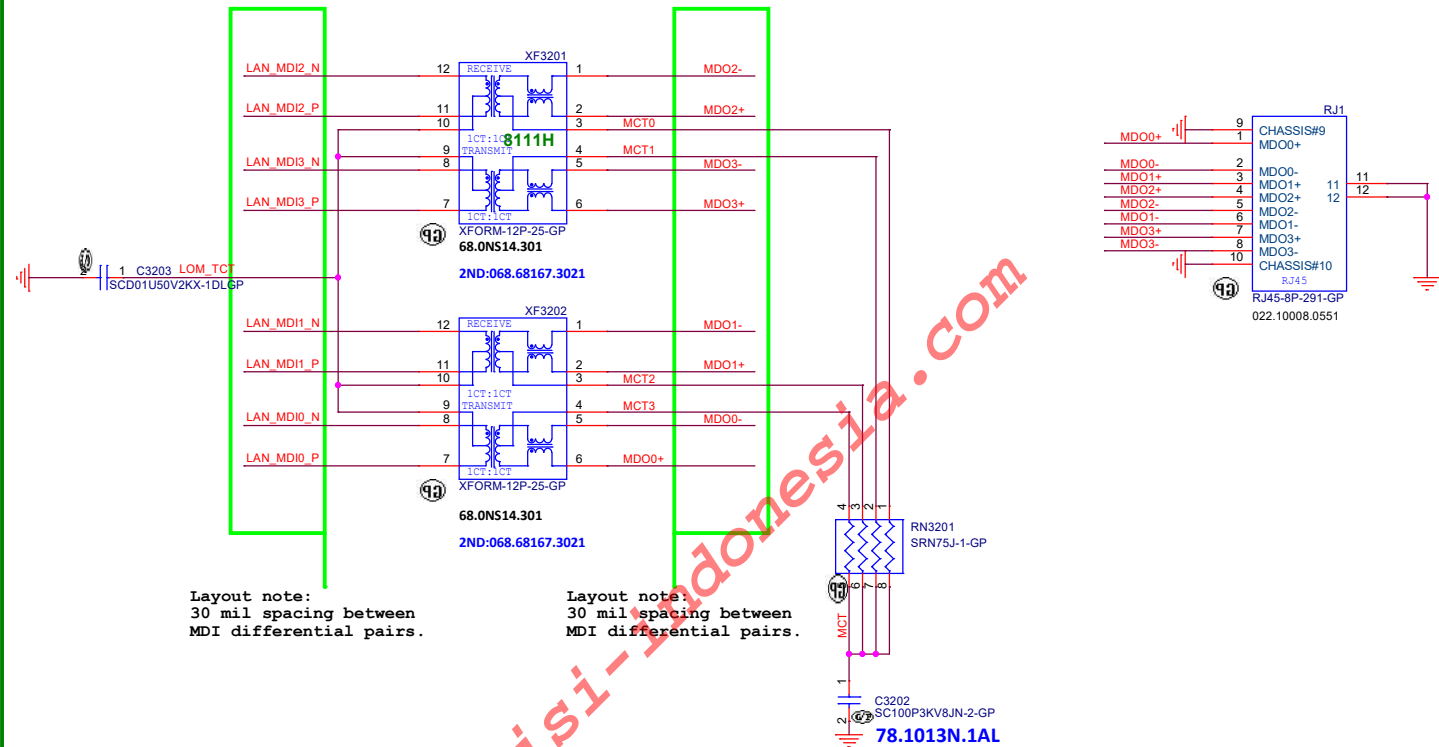
Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)

MDI

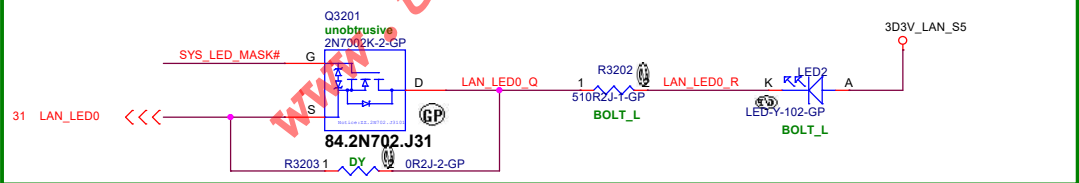


24,64 SYS\_LED\_MASK# >>>

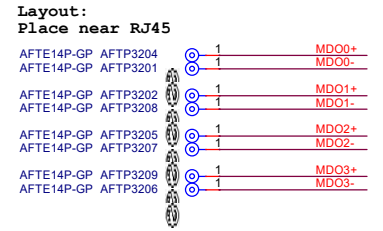


LED

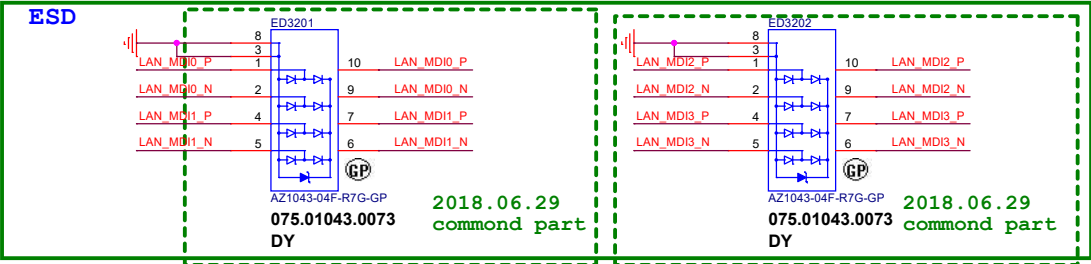
Green LED Status:  
Blinking:Data transmit (10/100/1000)  
Always Turn On: Network Connection exist  
Turn Off: No network connection exist



TEST PAD



ESD





(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Card Reader Re-driver</b>			
Size	Document Number		Rev
A2	<b>BOLT WHL</b>		A00
Date: Thursday, December 27, 2018			
Sheet 32		of 105	

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB2.0 CONN**

Size

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

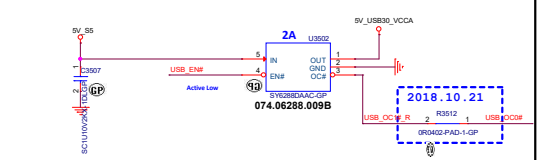
Sheet 34 of 105

Main Func = USB 3.0

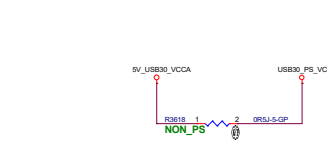
USB Power Switch Enable

24.66 USB\_EN# >>> \_\_\_\_\_  
16.36 USB\_OC# >>> \_\_\_\_\_

USB Power Switch



USB Power Sharing



3.1 阻值範圍:  $\geq 1\Omega$  &  $0\Omega$

型別	電壓 規格	電流 規格	電阻 規格	T.C.R (ppm/°C)	阻值範圍 E-24 ~ E-96	阻值範圍 E-24 ~ E-96	阻值範圍 E-24 ~ E-96	阻值範圍 E-24 ~ E-96	阻值範圍 E-24 ~ E-96	JUMPER (0Ω)	JUMPER (0Ω)	JUMPER (0Ω)
RT711 (0241)	1-W 2V	25V	50V	<200	—	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	0.5A	0.5A	50mΩ
RT712 (0402)	1-W 1V	50V	100V	<200	—	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	1A	1A	50mΩ
RT713 (0402)	1-W 1V	75V	150V	<200	—	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	2A	2A	50mΩ
RT714 (0402)	1-W 1V	150V	300V	<200	—	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	10.2R ~ 100	2A	2A	50mΩ

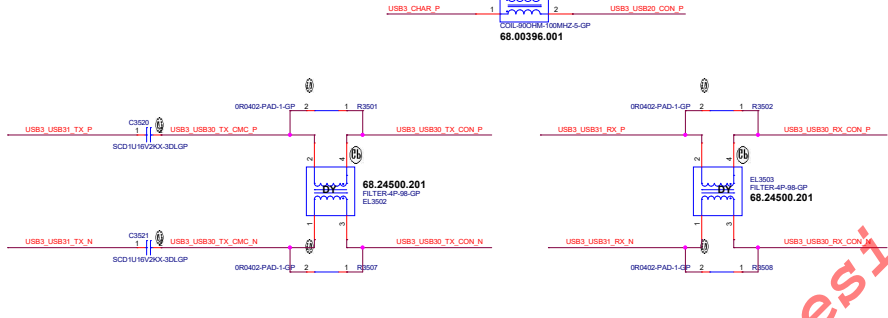
USB2.0 from USB Charger

36 USB2\_CHAR\_N <<> \_\_\_\_\_  
36 USB2\_CHAR\_P <<> \_\_\_\_\_

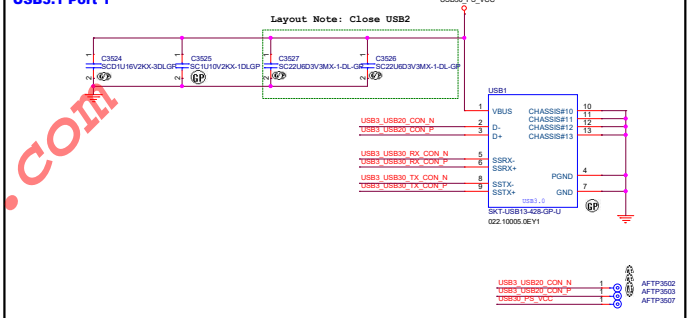
USB3.1

16 USB3\_USB31\_TX\_P >>> \_\_\_\_\_  
16 USB3\_USB31\_TX\_N >>> \_\_\_\_\_  
16 USB3\_USB31\_RX\_P >>> \_\_\_\_\_  
16 USB3\_USB31\_RX\_N >>> \_\_\_\_\_

CMC



USB-A Connector  
USB3.1 Port 1



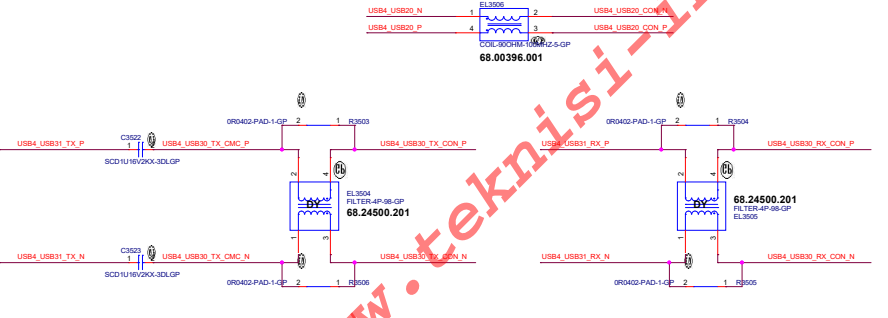
USB2.0

16 USB4\_USB20\_N <<> \_\_\_\_\_  
16 USB4\_USB20\_P <<> \_\_\_\_\_

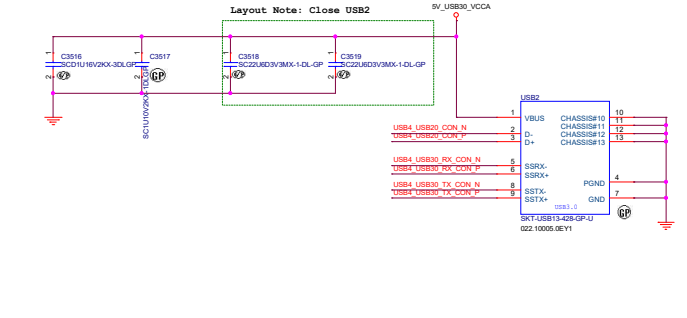
USB3.1

16 USB4\_USB31\_TX\_P >>> \_\_\_\_\_  
16 USB4\_USB31\_TX\_N >>> \_\_\_\_\_  
16 USB4\_USB31\_RX\_P >>> \_\_\_\_\_  
16 USB4\_USB31\_RX\_N >>> \_\_\_\_\_

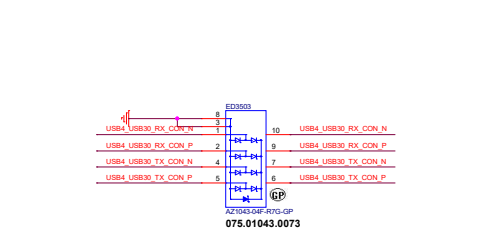
CMC



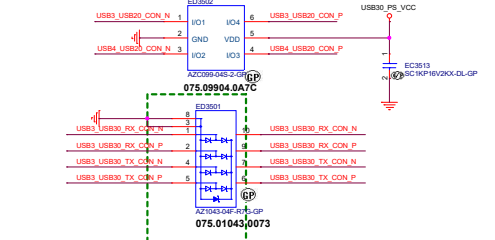
USB-A Connector  
USB3.1 Port 2



ESD FOR PORT1



ESD FOR PORT2

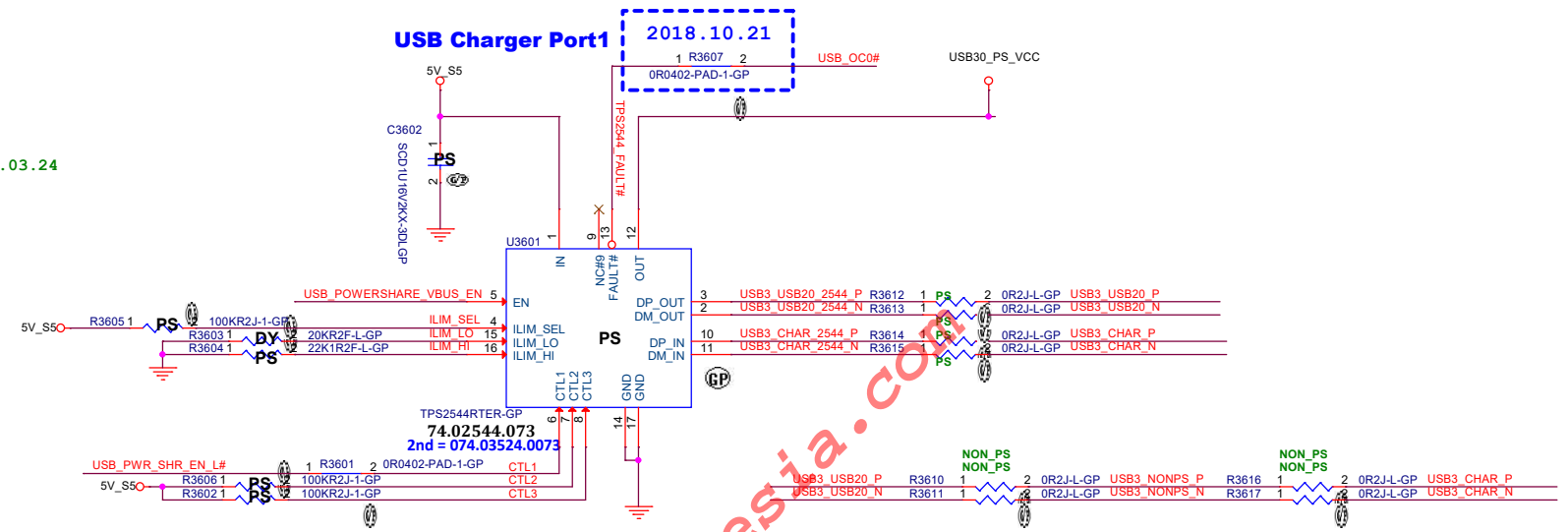


Main Func = USB Charger

2018.03.24

USB Charger Port1

2018.10.21



35 USB3\_CHAR\_P <<<<  
35 USB3\_CHAR\_N <<<<  
16 USB3\_USB20\_P <<<<  
16 USB3\_USB20\_N <<<<

24 USB\_POWERSHARE\_VBUS\_EN >>>>  
24 USB\_PWR\_SHR\_EN\_L# >>>>  
16,35 USB\_OC0# <<<<


Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_vp} (mA) = \frac{50,500}{(R_{ILIM\_XX} (k\Omega) + 0.1)}$$

R<sub>ILIM,XX</sub> corresponds to either R<sub>ILIM\_HI</sub> or R<sub>ILIM\_LO</sub> as appropriate.

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Charger**

Size: Custom	Document Number: <b>BOLT WHL</b>	Rev: <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 36 of 105

(Blanking)

www.teknisi-indonesia.com


BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB3.0 PORT</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date:	Thursday, December 27, 2018		Sheet 37 of 105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taippei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB3.1 GEN-2 Redriver</b>			
Size	Document Number	Rev	
A2	<b>BOLT WHL</b>	<b>A00</b>	
Date: Thursday, December 27, 2018		Sheet 38	of 105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(RSVD)			
Size	Document Number		Rev
A2	BOLT WHL		A00
Date: Thursday, December 27, 2018			
Sheet		39	of 105






(Blanking)

www.teknisi-indonesia.com


BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sequence (Modern Standby)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 41 of	105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

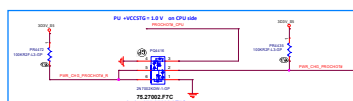
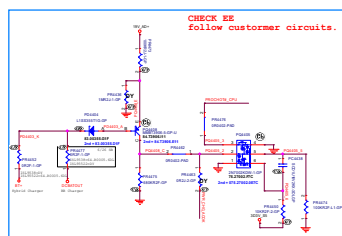
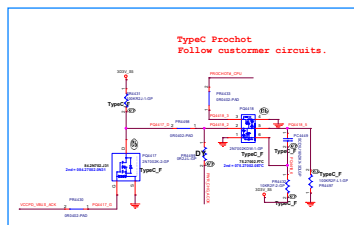
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Connected_Standby(2/2)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 42 of	105



## ISL95522 Hybrid Charger

## Default ISL9538 Buck-Boost Charger

OFF PAGE



## BOM Change List

ITEM	QTY	DESCRIPTION	REASON	DATE
1	1	ISL95522	NEW	2018-10-25
2	1	ISL9538	NEW	2018-10-25
3	1	ISL95522	NEW	2018-10-25
4	1	ISL9538	NEW	2018-10-25
5	1	ISL95522	NEW	2018-10-25
6	1	ISL9538	NEW	2018-10-25
7	1	ISL95522	NEW	2018-10-25
8	1	ISL9538	NEW	2018-10-25
9	1	ISL95522	NEW	2018-10-25
10	1	ISL9538	NEW	2018-10-25

## ISL9538

TABLE 33. PROG PIN PROGRAMMING OPTIONS

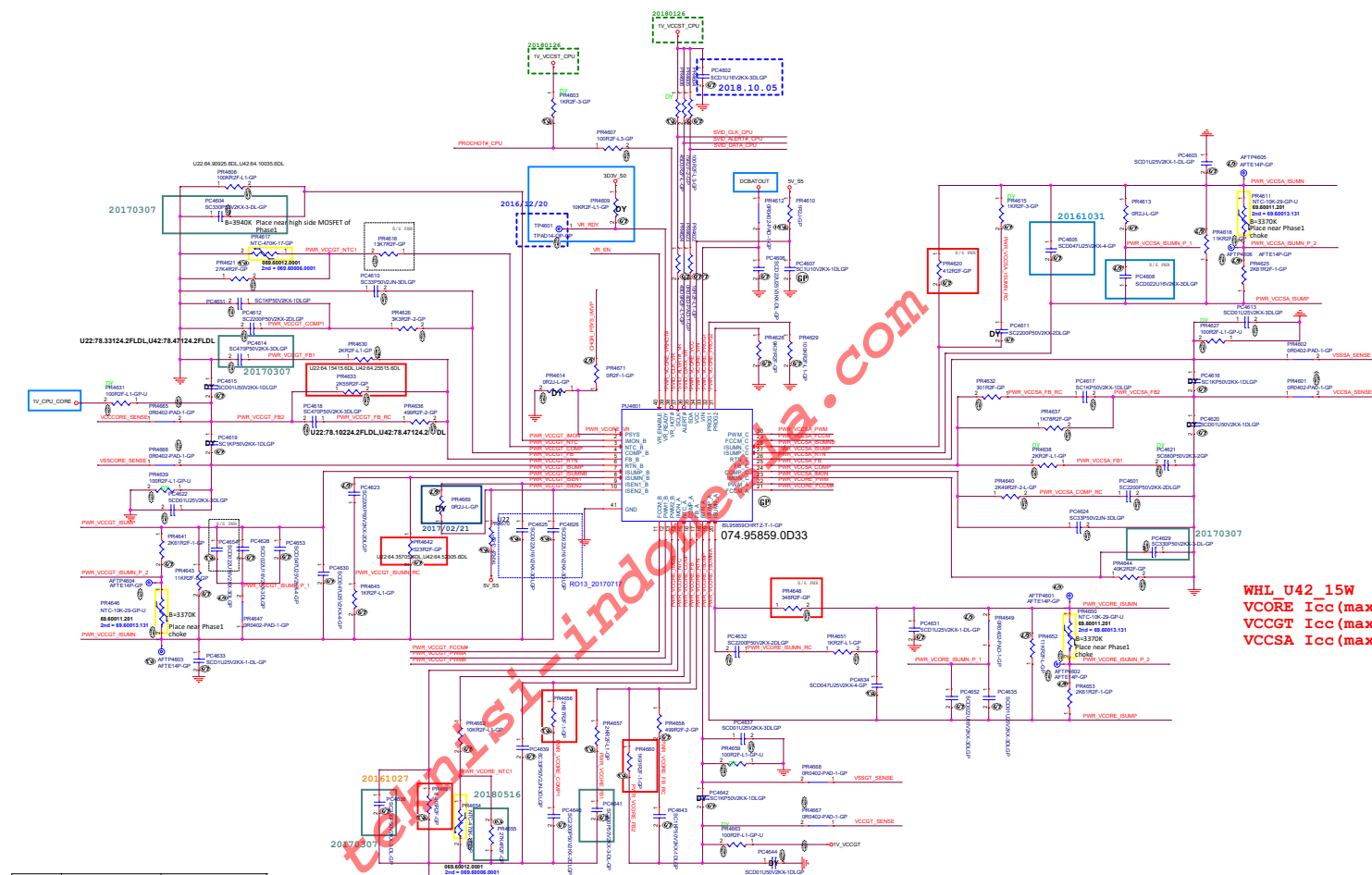
PROG PIN	MIN	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Default Actual charging	Default Actual R <sub>DS(on)</sub>
0	0	0	1	733kHz	No	0.47%
8,45	0	0	1	733kHz	No	1.5
14,7	0	0	1	1MHz	No	1.5
15,0	0	0	1	1MHz	No	0.47%
28,0	0	0	1	733kHz	Yes	0.47%
29,7	0	0	1	733kHz	Yes	1.5
33,2	0	0	1	733kHz	Yes	1.5
33,3	0	0	1	733kHz	Yes	0.47%
33,4	0	0	1	1MHz	No	0.47%
33,5	0	0	1	1MHz	No	1.5
33,6	0	0	1	733kHz	No	1.5
33,7	0	0	1	733kHz	No	0.47%
33,8	0	0	1	733kHz	No	1.5
33,9	0	0	1	733kHz	No	0.47%
33,10	0	0	1	733kHz	No	1.5
33,11	0	0	1	733kHz	No	0.47%
33,12	0	0	1	733kHz	No	1.5
33,13	0	0	1	733kHz	No	0.47%
33,14	0	0	1	733kHz	No	1.5
33,15	0	0	1	733kHz	No	0.47%
33,16	0	0	1	733kHz	No	1.5
33,17	0	0	1	733kHz	No	0.47%
33,18	0	0	1	733kHz	No	1.5
33,19	0	0	1	733kHz	No	0.47%
33,20	0	0	1	733kHz	No	1.5
33,21	0	0	1	733kHz	No	0.47%
33,22	0	0	1	733kHz	No	1.5
33,23	0	0	1	733kHz	No	0.47%
33,24	0	0	1	733kHz	No	1.5
33,25	0	0	1	733kHz	No	0.47%
33,26	0	0	1	733kHz	No	1.5
33,27	0	0	1	733kHz	No	0.47%
33,28	0	0	1	733kHz	No	1.5
33,29	0	0	1	733kHz	No	0.47%
33,30	0	0	1	733kHz	No	1.5
33,31	0	0	1	733kHz	No	0.47%
33,32	0	0	1	733kHz	No	1.5
33,33	0	0	1	733kHz	No	0.47%
33,34	0	0	1	733kHz	No	1.5
33,35	0	0	1	733kHz	No	0.47%
33,36	0	0	1	733kHz	No	1.5
33,37	0	0	1	733kHz	No	0.47%
33,38	0	0	1	733kHz	No	1.5
33,39	0	0	1	733kHz	No	0.47%
33,40	0	0	1	733kHz	No	1.5

## ISL95522

Table 34. Prog Pin Programming Options

Prog-GND Resistance (Ω)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
Typ (1% Standard Resistor)			
0	WDC	R <sub>CS</sub> = 2.1	3
22.6		R <sub>CS</sub> = 10mΩ	4
38.3		R <sub>CS</sub> = 5mΩ	2
		R <sub>CS</sub> = 20mΩ	
		R <sub>CS</sub> = 10mΩ	
66.6		R <sub>CS</sub> = 1.1	3
66.6		R <sub>CS</sub> = 10mΩ	4
102		R <sub>CS</sub> = 10mΩ	2
150		R <sub>CS</sub> = 20mΩ	4
150		R <sub>CS</sub> = 20mΩ	2
182		R <sub>CS</sub> = 20mΩ	3
215		R <sub>CS</sub> = 2.1	4
237		R <sub>CS</sub> = 10mΩ	2
255		R <sub>CS</sub> = 5mΩ	
		R <sub>CS</sub> = 20mΩ	
		R <sub>CS</sub> = 10mΩ	





48 PWR\_VCCGT\_BEN1 >>>  
48 PWR\_VCCGT\_BEN2 >>>

- 32A4 PROCHOT1-GP
- 1 VCCORE\_SENSE1
- 2 VCCORE\_SENSE2
- 3 VCCORE\_SENSE3
- 4 VCCORE\_SENSE4
- 5 VCCORE\_SENSE5
- 6 VCCORE\_SENSE6
- 7 VCCORE\_SENSE7
- 8 VCCORE\_SENSE8
- 9 VCCORE\_SENSE9
- 10 VCCORE\_SENSE10
- 11 VCCORE\_SENSE11
- 12 VCCORE\_SENSE12
- 13 VCCORE\_SENSE13
- 14 VCCORE\_SENSE14
- 15 VCCORE\_SENSE15
- 16 VCCORE\_SENSE16
- 17 VCCORE\_SENSE17
- 18 VCCORE\_SENSE18
- 19 VCCORE\_SENSE19
- 20 VCCORE\_SENSE20
- 21 VCCORE\_SENSE21
- 22 VCCORE\_SENSE22
- 23 VCCORE\_SENSE23
- 24 VCCORE\_SENSE24
- 25 VCCORE\_SENSE25
- 26 VCCORE\_SENSE26
- 27 VCCORE\_SENSE27
- 28 VCCORE\_SENSE28
- 29 VCCORE\_SENSE29
- 30 VCCORE\_SENSE30
- 31 VCCORE\_SENSE31
- 32 VCCORE\_SENSE32
- 33 VCCORE\_SENSE33
- 34 VCCORE\_SENSE34
- 35 VCCORE\_SENSE35
- 36 VCCORE\_SENSE36
- 37 VCCORE\_SENSE37
- 38 VCCORE\_SENSE38
- 39 VCCORE\_SENSE39
- 40 VCCORE\_SENSE40
- 41 VCCORE\_SENSE41
- 42 VCCORE\_SENSE42
- 43 VCCORE\_SENSE43
- 44 VCCORE\_SENSE44
- 45 VCCORE\_SENSE45
- 46 VCCORE\_SENSE46
- 47 VCCORE\_SENSE47
- 48 VCCORE\_SENSE48
- 49 VCCORE\_SENSE49
- 50 VCCORE\_SENSE50
- 51 VCCORE\_SENSE51
- 52 VCCORE\_SENSE52
- 53 VCCORE\_SENSE53
- 54 VCCORE\_SENSE54
- 55 VCCORE\_SENSE55
- 56 VCCORE\_SENSE56
- 57 VCCORE\_SENSE57
- 58 VCCORE\_SENSE58
- 59 VCCORE\_SENSE59
- 60 VCCORE\_SENSE60
- 61 VCCORE\_SENSE61
- 62 VCCORE\_SENSE62
- 63 VCCORE\_SENSE63
- 64 VCCORE\_SENSE64
- 65 VCCORE\_SENSE65
- 66 VCCORE\_SENSE66
- 67 VCCORE\_SENSE67
- 68 VCCORE\_SENSE68
- 69 VCCORE\_SENSE69
- 70 VCCORE\_SENSE70
- 71 VCCORE\_SENSE71
- 72 VCCORE\_SENSE72
- 73 VCCORE\_SENSE73
- 74 VCCORE\_SENSE74
- 75 VCCORE\_SENSE75
- 76 VCCORE\_SENSE76
- 77 VCCORE\_SENSE77
- 78 VCCORE\_SENSE78
- 79 VCCORE\_SENSE79
- 80 VCCORE\_SENSE80
- 81 VCCORE\_SENSE81
- 82 VCCORE\_SENSE82
- 83 VCCORE\_SENSE83
- 84 VCCORE\_SENSE84
- 85 VCCORE\_SENSE85
- 86 VCCORE\_SENSE86
- 87 VCCORE\_SENSE87
- 88 VCCORE\_SENSE88
- 89 VCCORE\_SENSE89
- 90 VCCORE\_SENSE90
- 91 VCCORE\_SENSE91
- 92 VCCORE\_SENSE92
- 93 VCCORE\_SENSE93
- 94 VCCORE\_SENSE94
- 95 VCCORE\_SENSE95
- 96 VCCORE\_SENSE96
- 97 VCCORE\_SENSE97
- 98 VCCORE\_SENSE98
- 99 VCCORE\_SENSE99
- 100 VCCORE\_SENSE100

	U22	U42	
PC4614	330p (78.33124.2FLDL)	470p (78.47124.2FLDL)	
PC4618	1Kp (78.10224.2FLDL)	470p (78.47124.2FLDL)	
PC4625	DY	0.022u (78.22321.2FLDL)	2017/08/25
PC4626	DY	0.022u (78.22321.2FLDL)	
PR4669	DY	DY	2017/02/21
PR4670	1K (64.10015.6DL)	DY	
PR4642	357 (64.35705.6DL)	523 (64.52305.6DL)	2018/04/27
PC4630	47nF (078.47322.02PD)	47nF (078.47322.02PD)	
PC4628	22nF (78.22321.2FLDL)	22nF (78.22321.2FLDL)	
PC4654	22nF (78.22321.2FLDL)	22nF (78.22321.2FLDL)	2018/08/06
PC4653	DY	47nF (078.47322.02PD)	
PR4633	1.54K (64.15415.6DL)	2.55K (64.25515.6DL)	
PR4608	90.9K (64.90925.6DL)	100K (64.10035.6DL)	2018/04/27

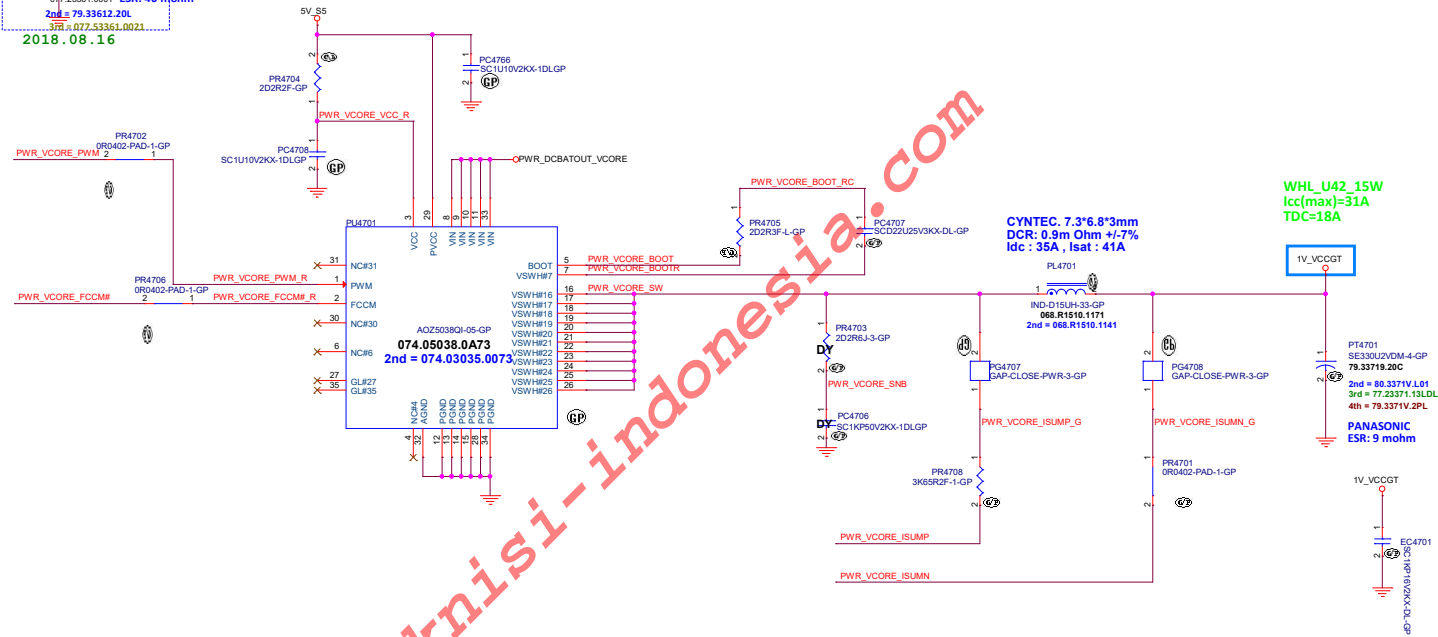
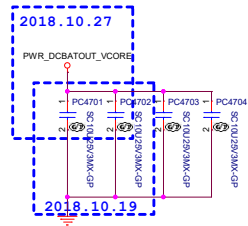
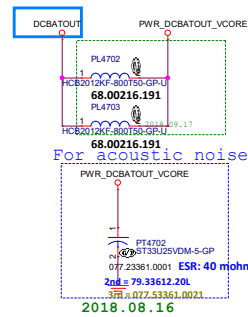
WHL\_U42\_15W  
VCCORE Icc(max)=70A TDC=48 A  
VCCGT Icc(max)=31A TDC=18 A  
VCCSA Icc(max)=6A TDC=4A



# Main FUNC = CPU CORE

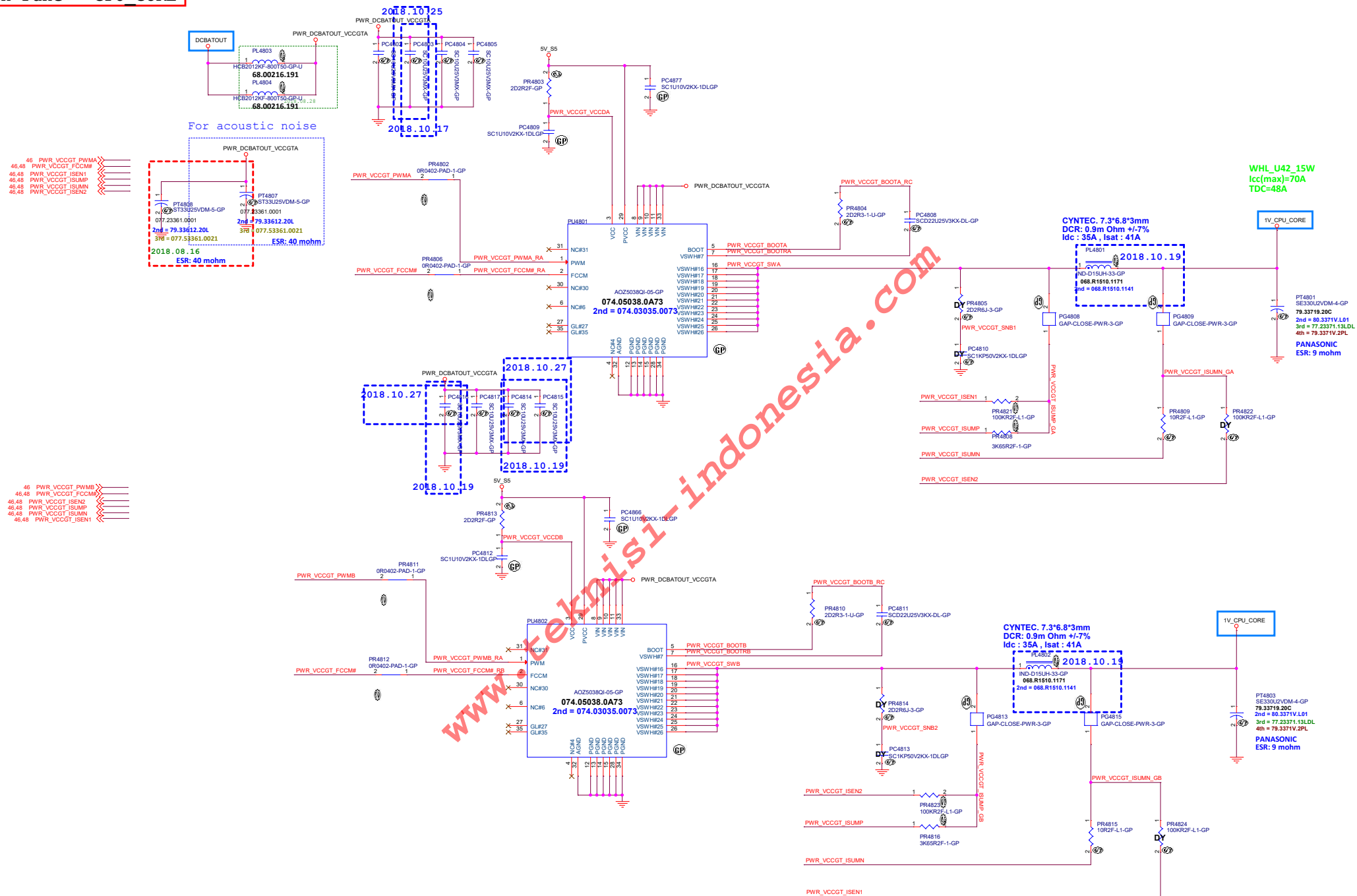
46 PWR\_VCORE\_PWM  
46 PWR\_VCORE\_FCCM  
46 PWR\_VCORE\_ISUMP  
46 PWR\_VCORE\_ISUMN

2018.09.17



BOLT 15 32bit 0822

**Main Func = CPU CORE**



**BOLT 15 32bit 0822**



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **NCP81382MN\_CPU\_VCCGT(3/3)**

Size A2	Document Number <b>BOLT WHL</b>	Rev A
------------	------------------------------------	----------

Date: Thursday, December 27, 2018 Sheet 48 of 106

Date:	Thursday, December 27, 2018	Sheet:	40	of	100
-------	-----------------------------	--------	----	----	-----

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

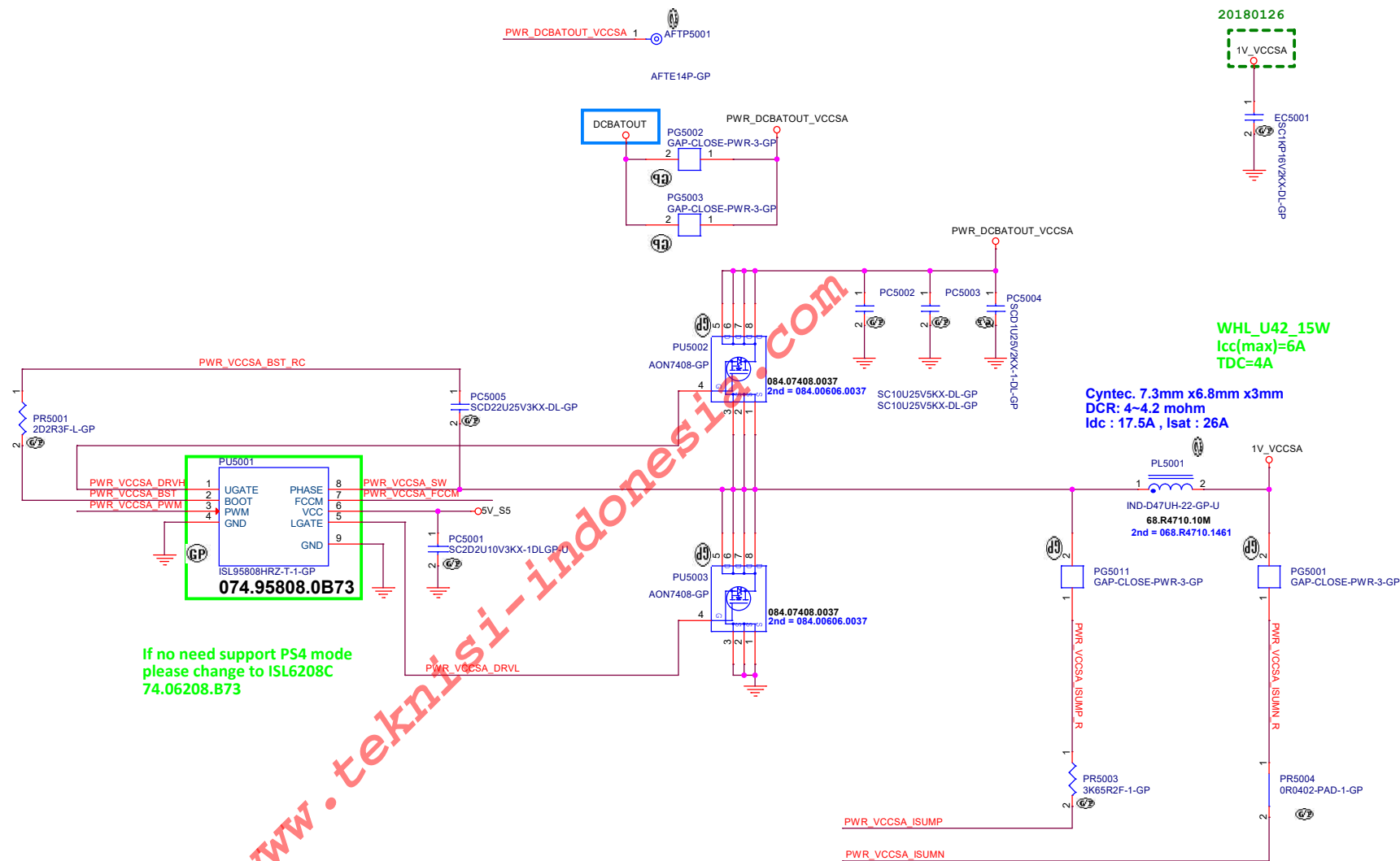
Title **NCP81210MN\_CPU\_VCCGTUS**

Size A4	Document Number <b>BOLT WHL</b>	Rev <b>A00</b>
------------	------------------------------------	-------------------

Date: Thursday, December 27, 2018 Sheet 49 of 106

Main FUNC = CPU\_CORE

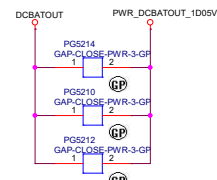
46 PWR\_VCCSA\_PWM  
46 PWR\_VCCSA\_FCCM  
46 PWR\_VCCSA\_ISUMP  
46 PWR\_VCCSA\_ISUMN



BOLT 15 32bit 0822

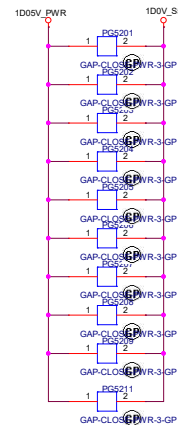
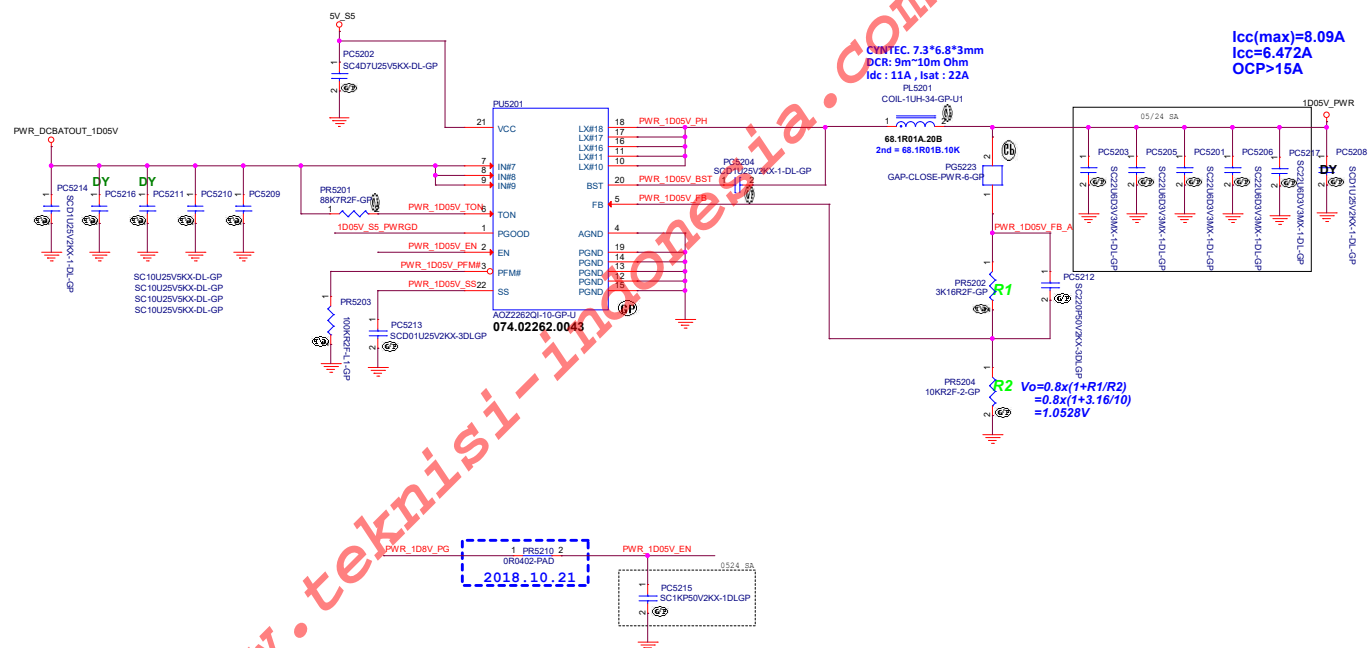
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: <b>VCCSA</b>			
Size: A3	Document Number: <b>BOLT WHL</b>	Rev: <b>A00</b>	
Date: Thursday, December 27, 2018	Sheet: 50	of	106





40 1D05V\_SS\_PWRGD <<<<  
53 PWR\_1D0V\_PG >>>>

## AOZ2262 for 1D05V

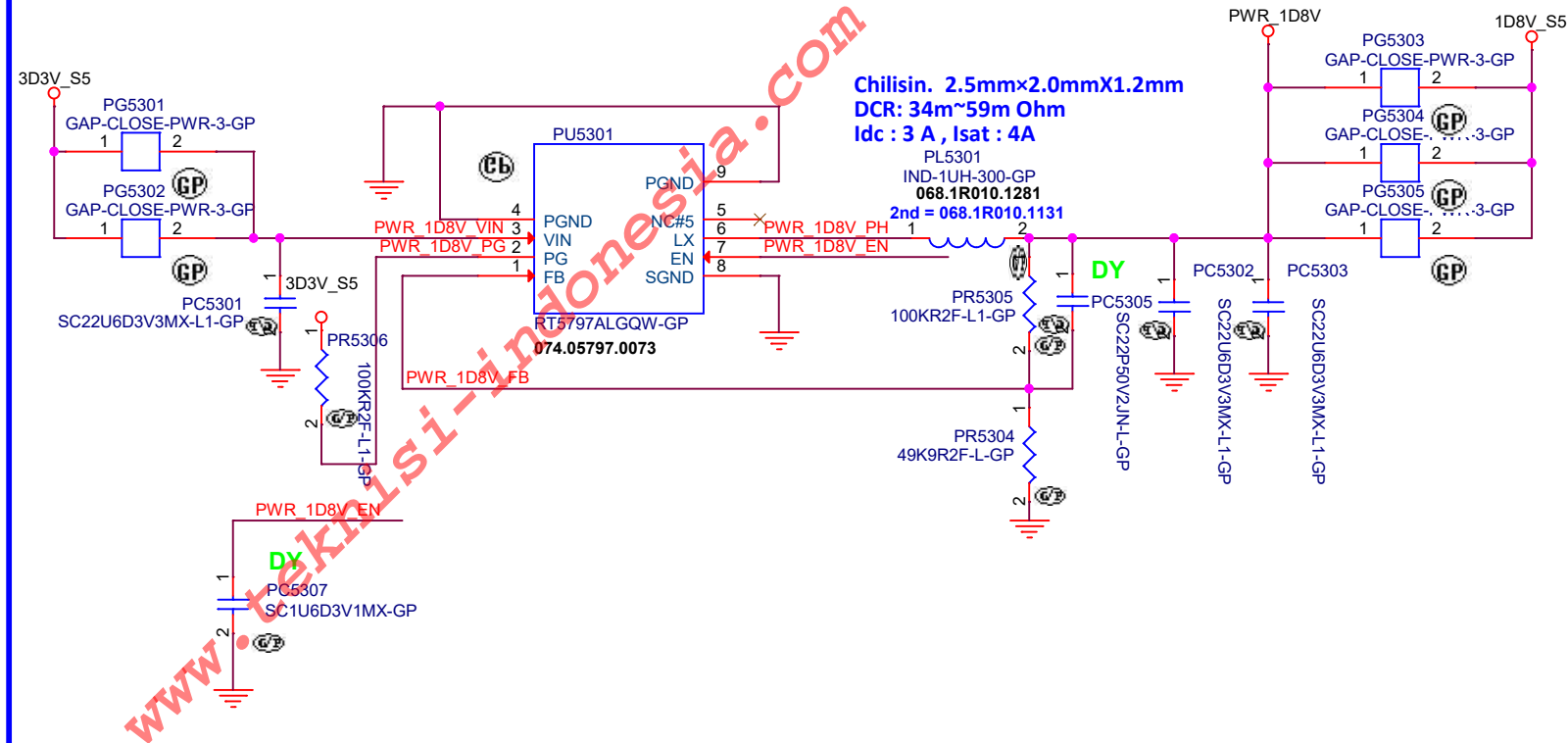
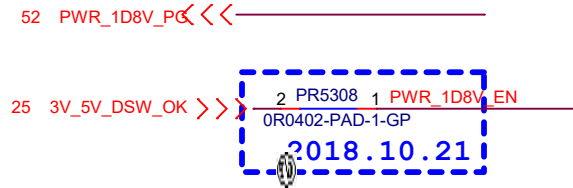


www.teknisi-indonesia.com

BOLT 15 32bit 0822

**Main Func = 1D8V**

lcc(max)=0.902A  
lcc=0.632A  
OCP>3A



BOLT 15 32bit 0822



## Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**1D8V**

Size	A4
------	----

Document Number
-----------------

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

Sheet 53 of 106


106



(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,  
Taippei Hsien 301, Taiwan, R.O.C.

Title

(Reserved)

Size

Document Number

Rev

Custom

BOLT WHL

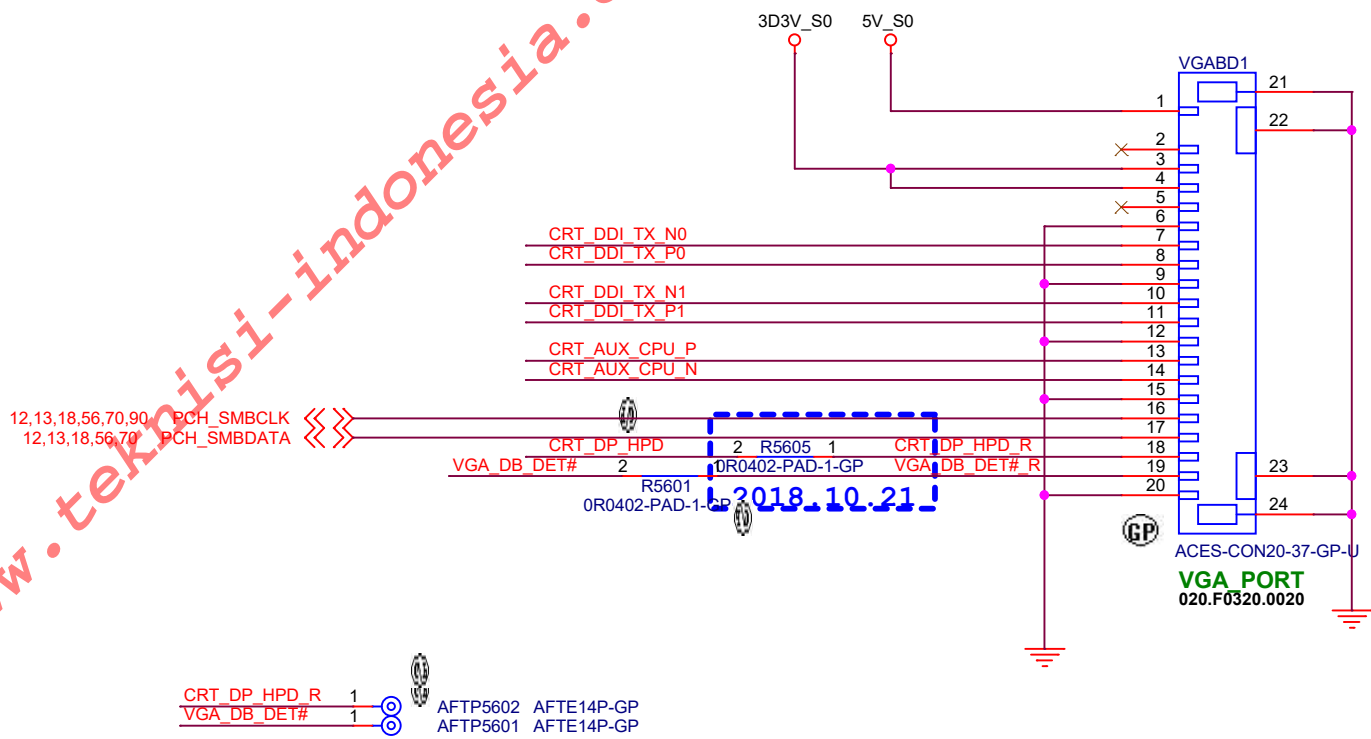
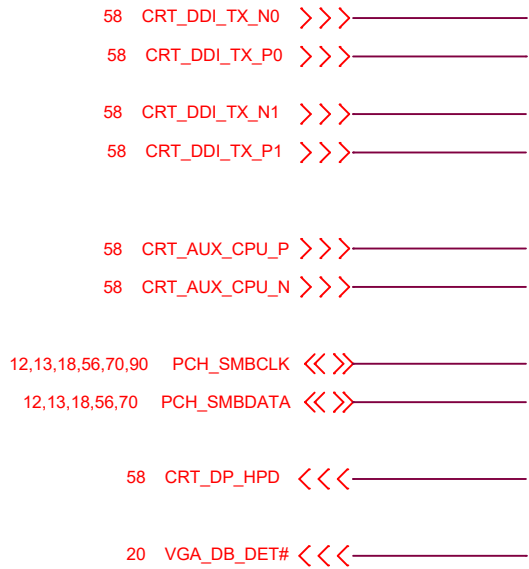
A00

Date: Thursday, December 27, 2018


Sheet 54 of 105



Main Func = CRT



BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CRT**

Size  
A4

Document Number  
**BOLT WHL**

Rev  
**A00**

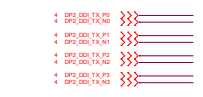
Date: Thursday, December 27, 2018

Sheet 56 of 105

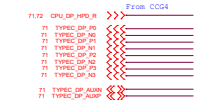


Main Func = DP Demux

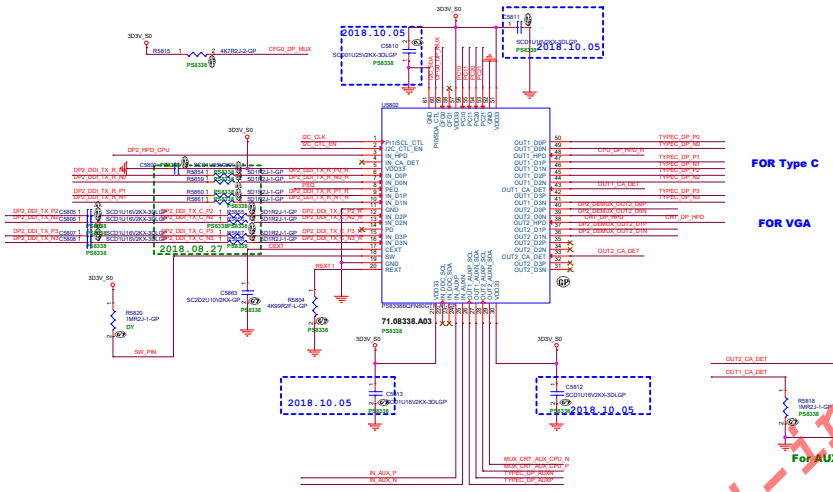
CPU DP to DP De-MUX



FOR Type C



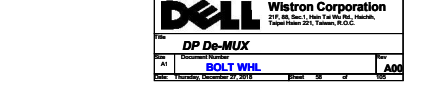
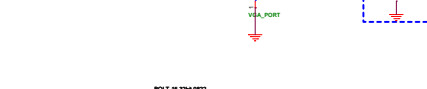
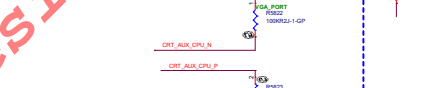
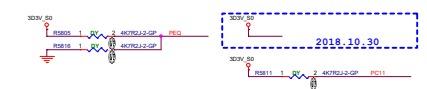
FOR VGA



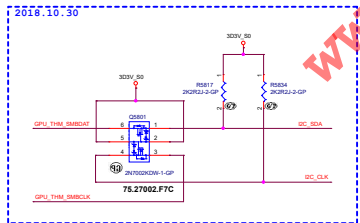
FOR Type C

FOR VGA

For AUX



SW	I/O	Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
		For Control Switching Mode (CFG0 = L):
		SW = L: Port1 is selected (default)
		SW = H: Port2 is selected
		For Automatic Switching Mode (CFG0 = H):
		SW = L: Port1 has higher priority when both ports are plugged (default)
		SW = H: Port2 has higher priority when both ports are plugged
		Overwritten by I2C register in I2C Control Mode



(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Main Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		(Reserved)	
Size	Document Number	Rev	
A2	BOLT WHL	A00	
Date: Thursday, December 27, 2018		Sheet 50	of 105

## HDD

```

16 HDD_SATA_TX_P11 >>> _____
16 HDD_SATA_TX_N11 >>> _____

16 HDD_SATA_RX_P1K <<< _____
16 HDD_SATA_RX_N1K <<< _____


70 FFS_INT2_Q >>> _____
16 HDD_DEVSLP >>> _____


18,20 HDD_DET# <<< _____

```

## 2018.08.08

HDD_SATA_TX_P11	C6028	1	SCD0125V2KX-3DLGP	HDD2_SATA_TX_CON_P
HDD_SATA_TX_N11	C6029	1	SCD0125V2KX-3DLGP	HDD2_SATA_TX_CON_N
HDD_SATA_RX_N11	C6030	1	SCD0125V2KX-3DLGP	HDD3_SATA_RX_CON_N
HDD_SATA_RX_P11	C6031	1	SCD0125V2KX-3DLGP	HDD2_SATA_RX_CON_P

Layout Note:  
Place near HDD2

Close to HD1

3 HDD\_SATA\_TX\_P11

4 HDD\_SATA\_TX\_N11

1 HDD\_SATA\_RX\_N11

2 HDD\_SATA\_RX\_P11

10

9

7

6

0628

AZ1043-04F-RTG-GP

075.01043.0073

DY

0628 change to command part

2018.06.29

020.K0222.0012  
2ND = 020.K0158.0012

ODD

```

16  ODD_SATA_TX_N12 >>>
16  ODD_SATA_TX_P12 >>>

16  ODD_SATA_RX_P12 <<<
16  ODD_SATA_RX_N12 <<<

16  SATA1_ODD_PRSENT# >>>

```

5V\_S0

1 R6003\_2  
R6003-PAD  
2018.10.21

5V\_000\_S0

C6018  
C10H10V2MX-DL-GU  
000

C6019  
C10H10V2MX-3D-LGI  
000

D6001  
SCD1U16V2KX-3D-LGI  
000

ODD\_SATA\_TX\_P12 SCD01U25V2KX-3DLGP D01  
 C6014 ODD\_SATA\_TX\_CON P 17  
 ODD\_SATA\_RX\_P12 SCD01U25V2KX-3DLGP D01  
 R6004 ODD\_SATA\_RX\_CON P 3  
 C6011 ODD\_SATA\_RX\_CON P 5  
 SATA\_ODD\_PRSNT# R 6  
 OR0402-PAD-1-GP 11  
 ODD\_S0 12  
 ODD\_TX 13  
 ODD\_RX 14  
 ODD\_PRSNT# 15  
 ODD\_TX 16  
 ODD\_RX 17  
 ODD\_PRSNT# 18  
 ODD\_S0 19  
 ODD\_TX 20  
 ODD\_RX 21  
 ODD\_PRSNT# 22  
 ODD\_TX 23  
 ODD\_RX 24  
 ODD\_PRSNT# 25  
 ODD\_S0 26  
 ODD\_TX 27  
 ODD\_RX 28  
 ODD\_PRSNT# 29  
 ODD\_TX 30  
 ODD\_RX 31  
 ODD\_PRSNT# 32  
 ODD\_S0 33  
 ODD\_TX 34  
 ODD\_RX 35  
 ODD\_PRSNT# 36  
 ODD\_TX 37  
 ODD\_RX 38  
 ODD\_PRSNT# 39  
 ODD\_S0 40  
 ODD\_TX 41  
 ODD\_RX 42  
 ODD\_PRSNT# 43  
 ODD\_TX 44  
 ODD\_RX 45  
 ODD\_PRSNT# 46  
 ODD\_S0 47  
 ODD\_TX 48  
 ODD\_RX 49  
 ODD\_PRSNT# 50  
 ODD\_TX 51  
 ODD\_RX 52  
 ODD\_PRSNT# 53  
 ODD\_S0 54  
 ODD\_TX 55  
 ODD\_RX 56  
 ODD\_PRSNT# 57  
 ODD\_TX 58  
 ODD\_RX 59  
 ODD\_PRSNT# 60  
 ODD\_S0 61  
 ODD\_TX 62  
 ODD\_RX 63  
 ODD\_PRSNT# 64  
 ODD\_TX 65  
 ODD\_RX 66  
 ODD\_PRSNT# 67  
 ODD\_S0 68  
 ODD\_TX 69  
 ODD\_RX 70  
 ODD\_PRSNT# 71  
 ODD\_TX 72  
 ODD\_RX 73  
 ODD\_PRSNT# 74  
 ODD\_S0 75  
 ODD\_TX 76  
 ODD\_RX 77  
 ODD\_PRSNT# 78  
 ODD\_TX 79  
 ODD\_RX 80  
 ODD\_PRSNT# 81  
 ODD\_S0 82  
 ODD\_TX 83  
 ODD\_RX 84  
 ODD\_PRSNT# 85  
 ODD\_TX 86  
 ODD\_RX 87  
 ODD\_PRSNT# 88  
 ODD\_S0 89  
 ODD\_TX 90  
 ODD\_RX 91  
 ODD\_PRSNT# 92  
 ODD\_TX 93  
 ODD\_RX 94  
 ODD\_PRSNT# 95  
 ODD\_S0 96  
 ODD\_TX 97  
 ODD\_RX 98  
 ODD\_PRSNT# 99  
 ODD\_TX 100  
 ODD\_RX 101  
 ODD\_PRSNT# 102  
 ODD\_S0 103  
 ODD\_TX 104  
 ODD\_RX 105  
 ODD\_PRSNT# 106  
 ODD\_TX 107  
 ODD\_RX 108  
 ODD\_PRSNT# 109  
 ODD\_S0 110  
 ODD\_TX 111  
 ODD\_RX 112  
 ODD\_PRSNT# 113  
 ODD\_TX 114  
 ODD\_RX 115  
 ODD\_PRSNT# 116  
 ODD\_S0 117  
 ODD\_TX 118  
 ODD\_RX 119  
 ODD\_PRSNT# 120  
 ODD\_TX 121  
 ODD\_RX 122  
 ODD\_PRSNT# 123  
 ODD\_S0 124  
 ODD\_TX 125  
 ODD\_RX 126  
 ODD\_PRSNT# 127  
 ODD\_TX 128  
 ODD\_RX 129  
 ODD\_PRSNT# 130  
 ODD\_S0 131  
 ODD\_TX 132  
 ODD\_RX 133  
 ODD\_PRSNT# 134  
 ODD\_TX 135  
 ODD\_RX 136  
 ODD\_PRSNT# 137  
 ODD\_S0 138  
 ODD\_TX 139  
 ODD\_RX 140  
 ODD\_PRSNT# 141  
 ODD\_TX 142  
 ODD\_RX 143  
 ODD\_PRSNT# 144  
 ODD\_S0 145  
 ODD\_TX 146  
 ODD\_RX 147  
 ODD\_PRSNT# 148  
 ODD\_TX 149  
 ODD\_RX 150  
 ODD\_PRSNT# 151  
 ODD\_S0 152  
 ODD\_TX 153  
 ODD\_RX 154  
 ODD\_PRSNT# 155  
 ODD\_TX 156  
 ODD\_RX 157  
 ODD\_PRSNT# 158  
 ODD\_S0 159  
 ODD\_TX 160  
 ODD\_RX 161  
 ODD\_PRSNT# 162  
 ODD\_TX 163  
 ODD\_RX 164  
 ODD\_PRSNT# 165  
 ODD\_S0 166  
 ODD\_TX 167  
 ODD\_RX 168  
 ODD\_PRSNT# 169  
 ODD\_TX 170  
 ODD\_RX 171  
 ODD\_PRSNT# 172  
 ODD\_S0 173  
 ODD\_TX 174  
 ODD\_RX 175  
 ODD\_PRSNT# 176  
 ODD\_TX 177  
 ODD\_RX 178  
 ODD\_PRSNT# 179  
 ODD\_S0 180  
 ODD\_TX 181  
 ODD\_RX 182  
 ODD\_PRSNT# 183  
 ODD\_TX 184  
 ODD\_RX 185  
 ODD\_PRSNT# 186  
 ODD\_S0 187  
 ODD\_TX 188  
 ODD\_RX 189  
 ODD\_PRSNT# 190  
 ODD\_TX 191  
 ODD\_RX 192  
 ODD\_PRSNT# 193  
 ODD\_S0 194  
 ODD\_TX 195  
 ODD\_RX 196  
 ODD\_PRSNT# 197  
 ODD\_TX 198  
 ODD\_RX 199  
 ODD\_PRSNT# 200  
 ODD\_S0 201  
 ODD\_TX 202  
 ODD\_RX 203  
 ODD\_PRSNT# 204  
 ODD\_TX 205  
 ODD\_RX 206  
 ODD\_PRSNT# 207  
 ODD\_S0 208  
 ODD\_TX 209  
 ODD\_RX 210  
 ODD\_PRSNT# 211  
 ODD\_TX 212  
 ODD\_RX 213  
 ODD\_PRSNT# 214  
 ODD\_S0 215  
 ODD\_TX 216  
 ODD\_RX 217  
 ODD\_PRSNT# 218  
 ODD\_TX 219  
 ODD\_RX 220  
 ODD\_PRSNT# 221  
 ODD\_S0 222  
 ODD\_TX 223  
 ODD\_RX 224  
 ODD\_PRSNT# 225  
 ODD\_TX 226  
 ODD\_RX 227  
 ODD\_PRSNT# 228  
 ODD\_S0 229  
 ODD\_TX 230  
 ODD\_RX 231  
 ODD\_PRSNT# 232  
 ODD\_TX 233  
 ODD\_RX 234  
 ODD\_PRSNT# 235  
 ODD\_S0 236  
 ODD\_TX 237  
 ODD\_RX 238  
 ODD\_PRSNT# 239  
 ODD\_TX 240  
 ODD\_RX 241  
 ODD\_PRSNT# 242  
 ODD\_S0 243  
 ODD\_TX 244  
 ODD\_RX 245  
 ODD\_PRSNT# 246  
 ODD\_TX 247  
 ODD\_RX 248  
 ODD\_PRSNT# 249  
 ODD\_S0 250  
 ODD\_TX 251  
 ODD\_RX 252  
 ODD\_PRSNT# 253  
 ODD\_TX 254  
 ODD\_RX 255  
 ODD\_PRSNT# 256  
 ODD\_S0 257  
 ODD\_TX 258  
 ODD\_RX 259  
 ODD\_PRSNT# 260  
 ODD\_TX 261  
 ODD\_RX 262  
 ODD\_PRSNT# 263  
 ODD\_S0 264  
 ODD\_TX 265  
 ODD\_RX 266  
 ODD\_PRSNT# 267  
 ODD\_TX 268  
 ODD\_RX 269  
 ODD\_PRSNT# 270  
 ODD\_S0 271  
 ODD\_TX 272  
 ODD\_RX 273  
 ODD\_PRSNT# 274  
 ODD\_TX 275  
 ODD\_RX 276  
 ODD\_PRSNT# 277  
 ODD\_S0 278  
 ODD\_TX 279  
 ODD\_RX 280  
 ODD\_PRSNT# 281  
 ODD\_TX 282  
 ODD\_RX 283  
 ODD\_PRSNT# 284  
 ODD\_S0 285  
 ODD\_TX 286  
 ODD\_RX 287  
 ODD\_PRSNT# 288  
 ODD\_TX 289  
 ODD\_RX 290  
 ODD\_PRSNT# 291  
 ODD\_S0 292  
 ODD\_TX 293  
 ODD\_RX 294  
 ODD\_PRSNT# 295  
 ODD\_TX 296  
 ODD\_RX 297  
 ODD\_PRSNT# 298  
 ODD\_S0 299  
 ODD\_TX 300  
 ODD\_RX 301  
 ODD\_PRSNT# 302  
 ODD\_TX 303  
 ODD\_RX 304  
 ODD\_PRSNT# 305  
 ODD\_S0 306  
 ODD\_TX 307  
 ODD\_RX 308  
 ODD\_PRSNT# 309  
 ODD\_TX 310  
 ODD\_RX 311  
 ODD\_PRSNT# 312  
 ODD\_S0 313  
 ODD\_TX 314  
 ODD\_RX 315  
 ODD\_PRSNT# 316  
 ODD\_TX 317  
 ODD\_RX 318  
 ODD\_PRSNT# 319  
 ODD\_S0 320  
 ODD\_TX 321  
 ODD\_RX 322  
 ODD\_PRSNT# 323  
 ODD\_TX 324  
 ODD\_RX 325  
 ODD\_PRSNT# 326  
 ODD\_S0 327  
 ODD\_TX 328  
 ODD\_RX 329  
 ODD\_PRSNT# 330  
 ODD\_TX 331  
 ODD\_RX 332  
 ODD\_PRSNT# 333  
 ODD\_S0 334  
 ODD\_TX 335  
 ODD\_RX 33

BOLT 15 32bit 0822



Main FUNC = WLAN

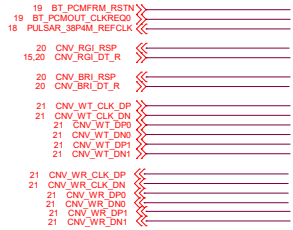
## BT



## WLAN



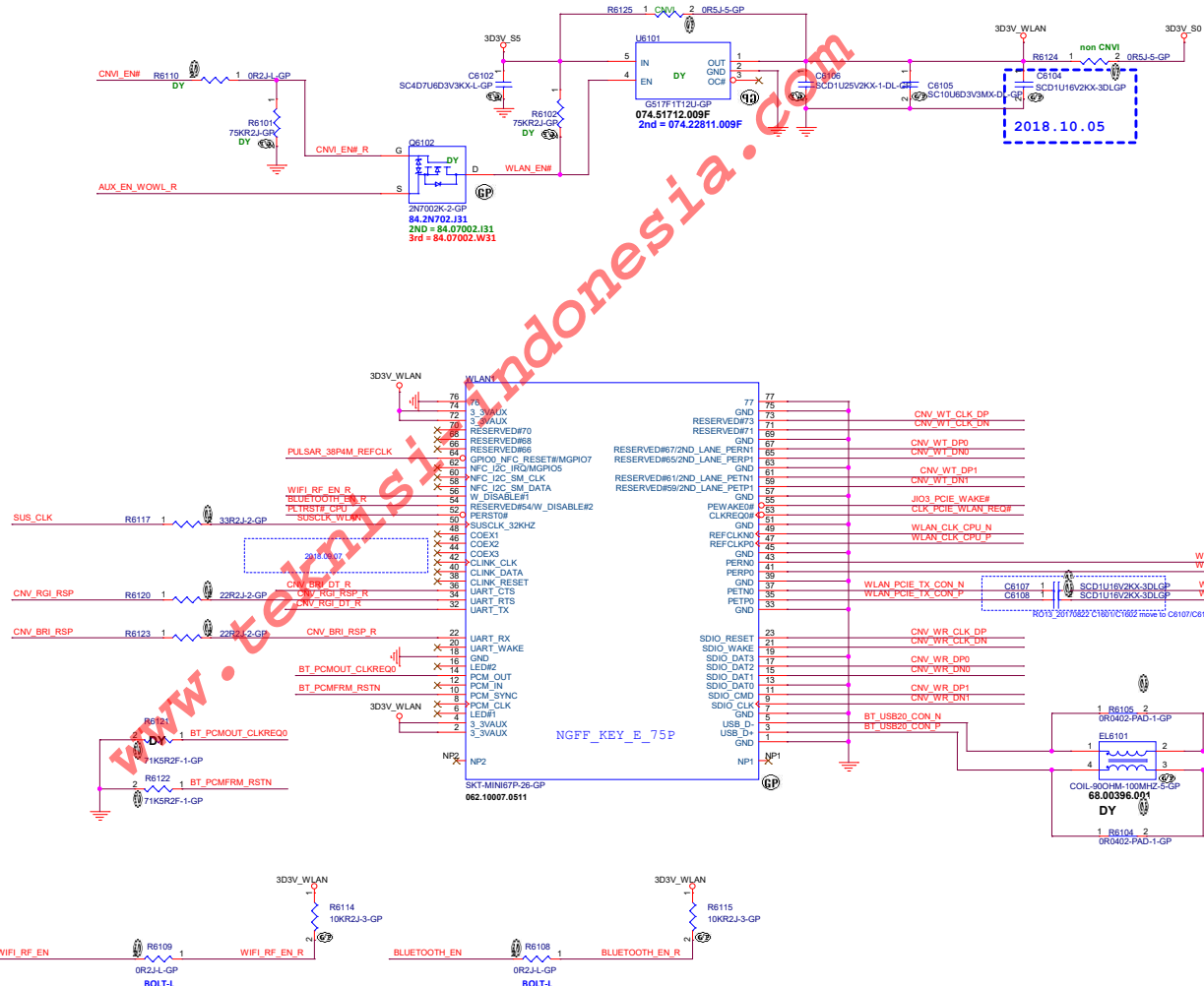
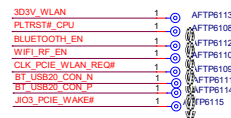
## CNVI



## Others



CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN



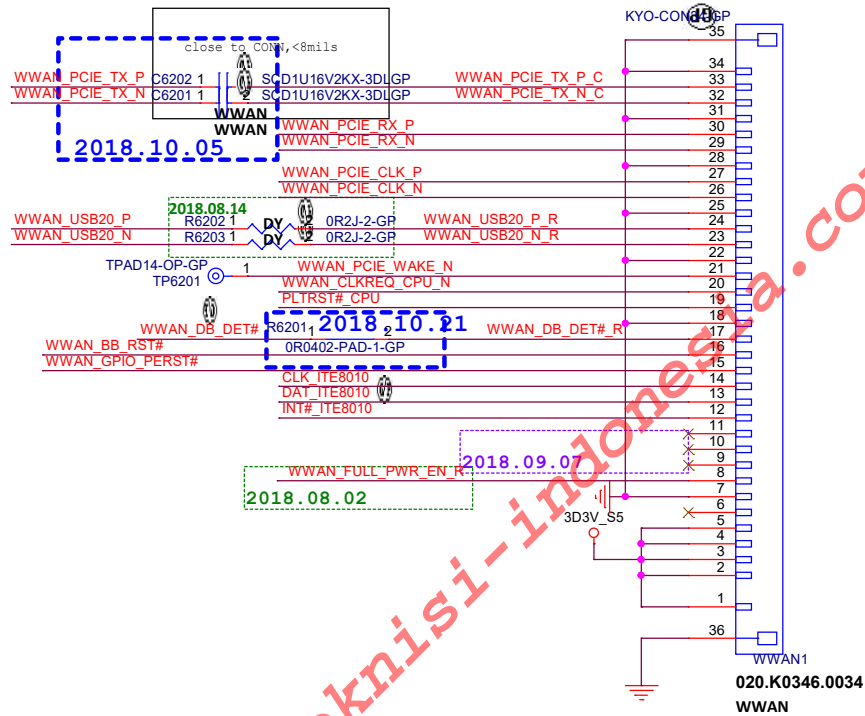
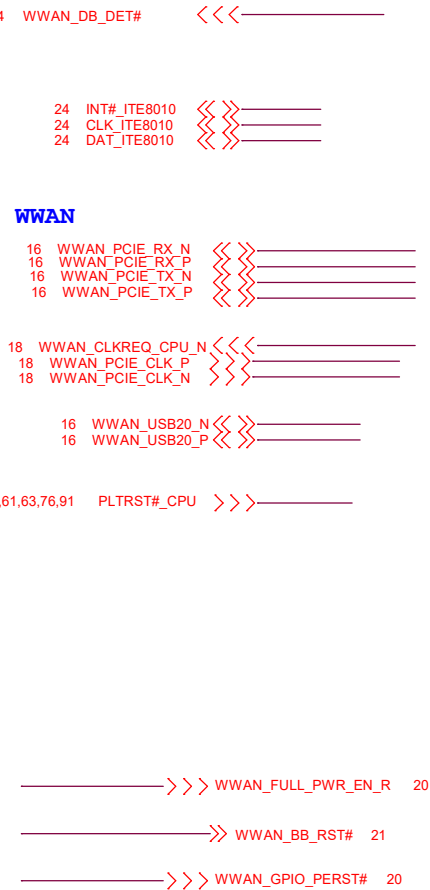
BOLT 15 32bit 0822



Title **NOFF W/AN CONN**

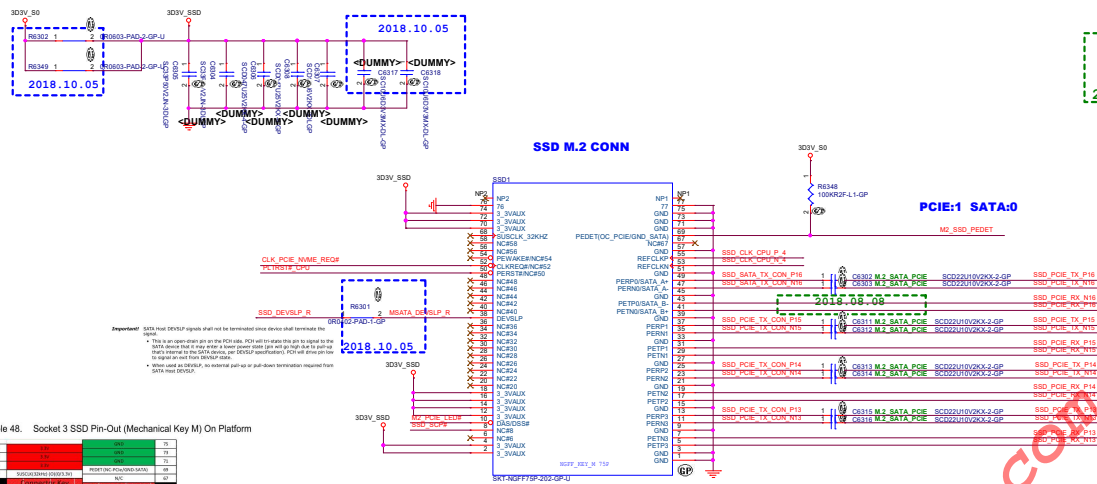
Size A2	Document Number <b>BOLT WHL</b>	Rev <b>A0</b>
Date: Thursday, December 27, 2018	Sheet 61 of	106

# Main FUNC = WWAN



BOLT 15 32bit 0822

<b>DELL</b>			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>WWAN</b>					
Size Custom	Document Number <b>BOLT WHL</b>				Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 62 of 105			

[illegible][illegible]

Condition	PCIe Gen2* Gen 2 Only	PCIe Gen3* Gen 3 Only	SATA Only	PCIe Express* Gen 2 / SATA	PCIe Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 1x and 10x nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen2\* SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor, and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices**
- Design Constraint: For PCIe\* Gen3\* SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices**

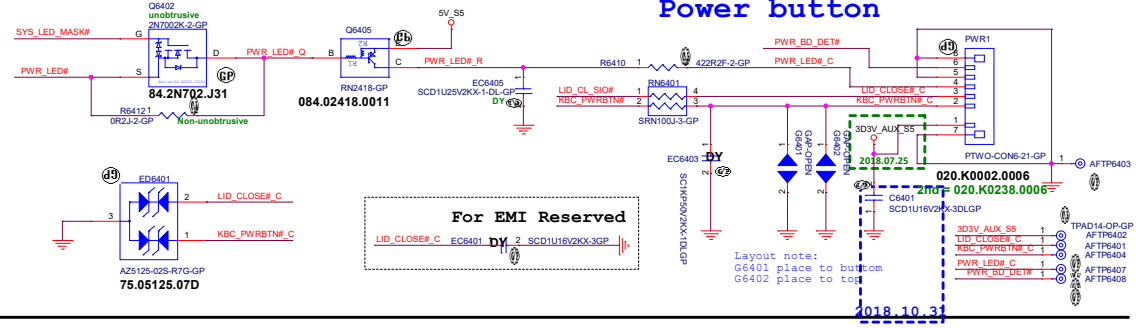
Design Constraints, Recommendations, and Notes for the "General Signal Integrity Signals Design Guidelines" are provided in the additional guidelines in this section for all design optimization guidelines.

Design Constraint: For PCIe\* lane that needs to support either **PCIe\* Gen2 devices** or **PCIe\* Gen3 devices**, follow the PCIe\* Gen 3 / SATA SATA multiplexed configuration. This option requires a 220 nF capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Main Func = Power BTN

24 PWR\_LED# >>> \_\_\_\_\_  
20.21 PWR\_BO\_DET# <<< \_\_\_\_\_  
24.92 LID\_CL\_SIO# <<< \_\_\_\_\_  
24.92 KBC\_PWRBTN# <<< \_\_\_\_\_

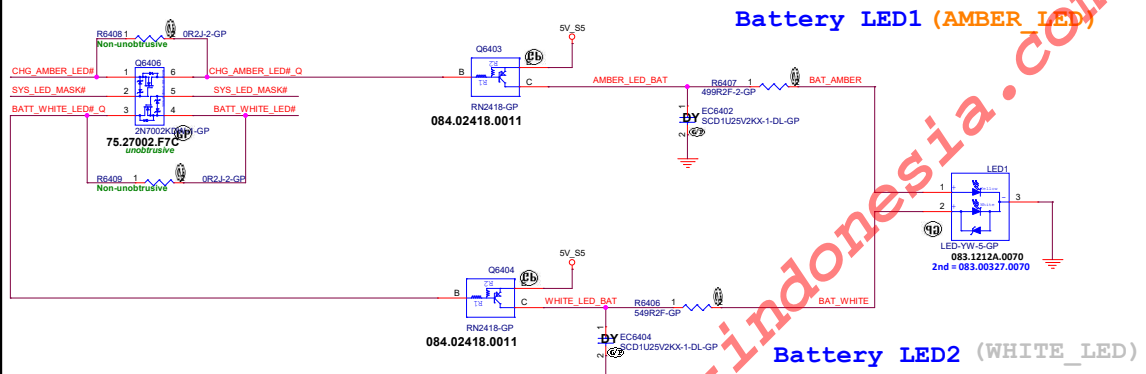
NONE FINGER PRINT 才會上件



Main Func = Battery LED

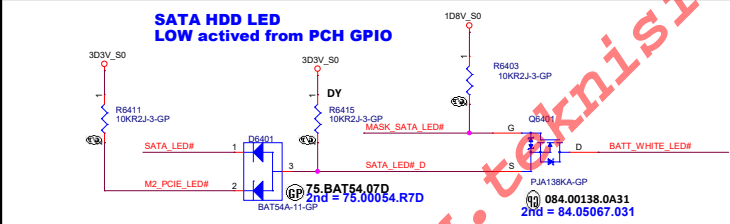
Low activated from KBC GPIO

24.32 SYS\_LED\_MASK# >>> \_\_\_\_\_  
24 CHG\_AMBER\_LED# >>> \_\_\_\_\_  
24 BATT\_WHITE\_LED# >>> \_\_\_\_\_



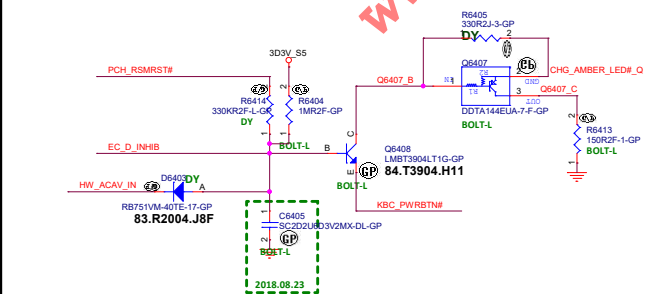
Main Func = HDD LED

24 MASK\_SATA\_LED# >>> \_\_\_\_\_  
16 SATA\_LED# >>> \_\_\_\_\_  
63 M2\_PCIE\_LED# <<< \_\_\_\_\_



Main Func = M-BIST

17.24 PCH\_RSMRST# >>> \_\_\_\_\_  
24 EC\_D\_IN#B >>> \_\_\_\_\_  
24.43.44 HW\_ACAV\_IN >>> \_\_\_\_\_



M-BIST(Mainboard Built-in Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

24 CAP\_LED#\_R >>>

24 KSII[0..7] >>>

24 KSQ[0..16] <<<

20 KB\_DET# <<<

KB\_LED\_BI\_DET <<<

24 KB\_LED\_PWM >>>

[illegible][illegible]

24 TP\_EN# >>> \_\_\_\_\_

24 CLK\_TP\_SIO <<< \_\_\_\_\_  
24 DAT\_TP\_SIO <<< \_\_\_\_\_

I2C0\_SCL\_TCH\_PAD >>> \_\_\_\_\_  
I2C0\_SDA\_TCH\_PAD >>> \_\_\_\_\_

24 TP\_WAKE\_KBC# <<< \_\_\_\_\_

24 PTP\_DIS# >>> \_\_\_\_\_

[illegible]

TP side has pull high

TP\_WAKE\_KBC# 1 R6511 2 TP\_VDD

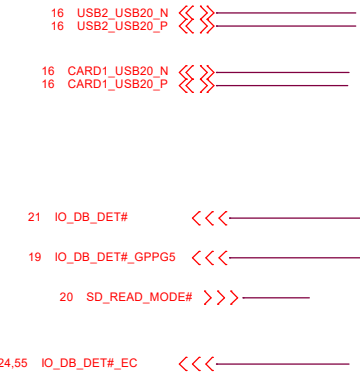
10KR2J-3-GR

TP\_WAKE

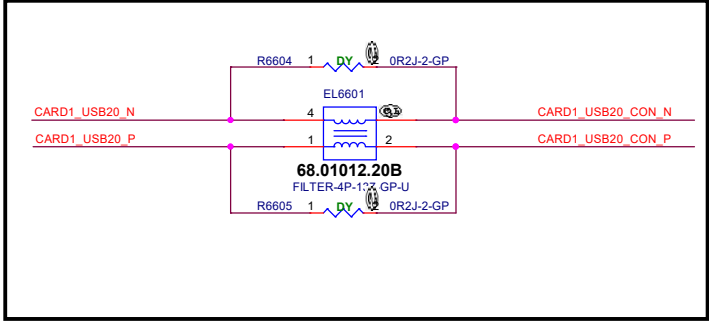
Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPTO
7	DAT (PS2)
8	CLK (PS2)

Main Func = IO Connector

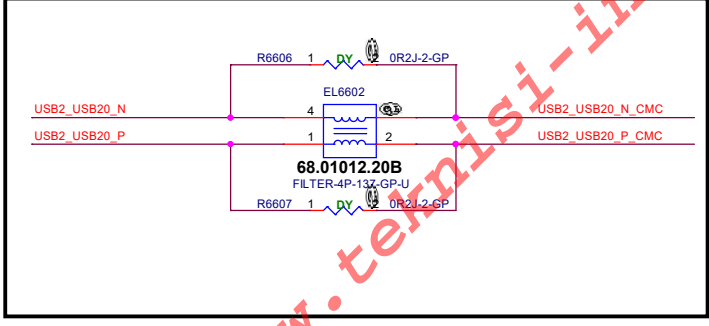
USB 2.0



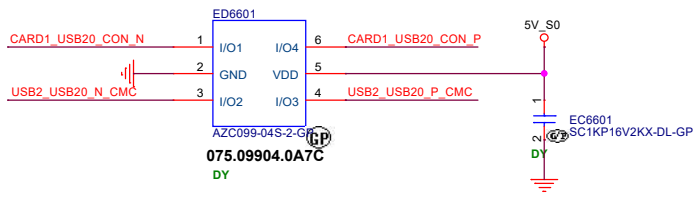
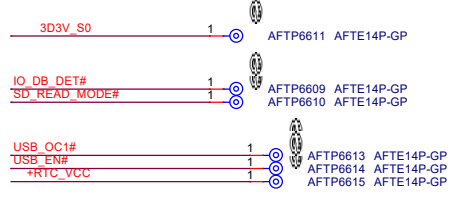
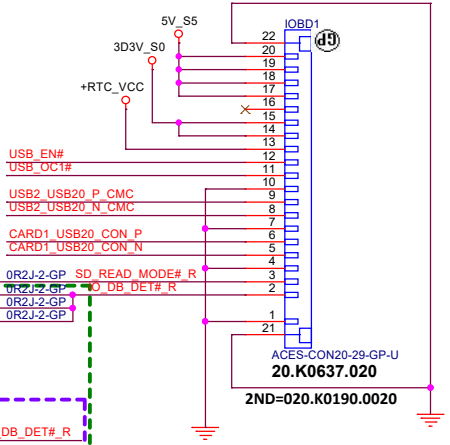
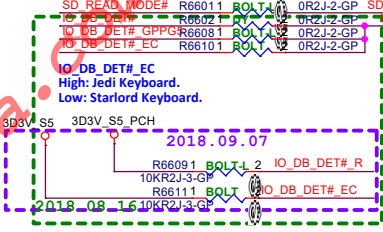
USB2.0 CARD



USB2.0 CARD



USB2.0 Card Reader SD3.0



USB OC



USB Switch Enable



BOLT 15 32bit 0822

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size	Document Number	Rev
Custom	<b>BOLT WHL</b>	<b>A00</b>
Date:	Thursday, December 27, 2018	Sheet 66 of 105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

Sheet 67 of 105

# Main Func = Debug

18,24 ESPI\_CLK  
18,24 ESPI\_RESET#  
18,24 ESPI\_CS#

24 HOST\_DEBUG\_TX

20 UART\_2\_CTXD\_DRXD  
20 UART\_2\_CRXD\_DTXD

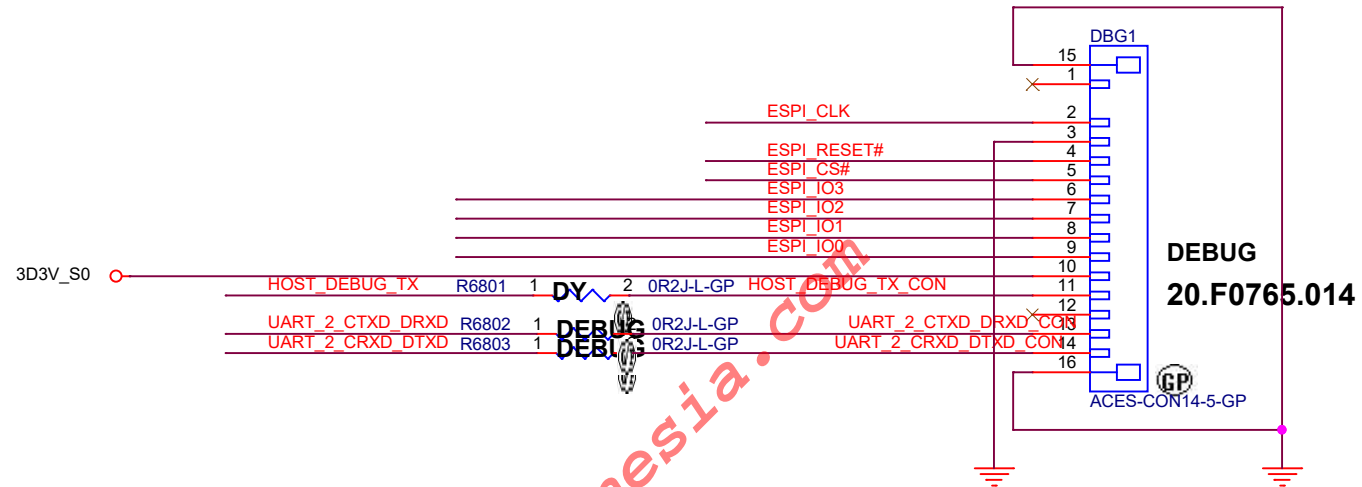
18,24 ESPI\_IO[3..0]

ESPI\_IO3  
ESPI\_IO1  
ESPI\_IO2  
ESPI\_IO0

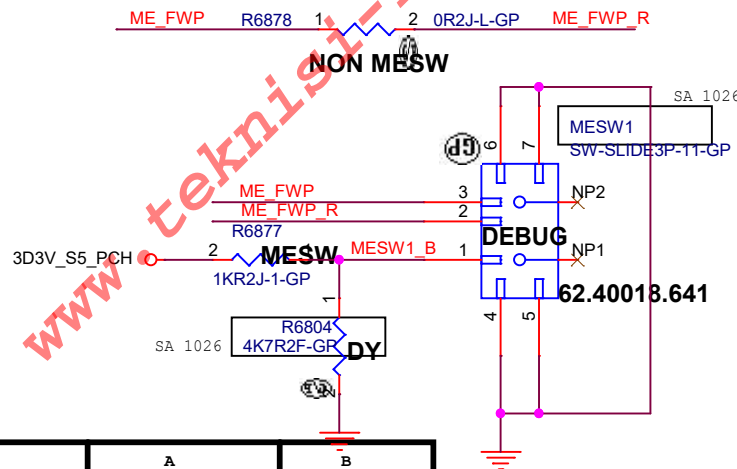
24 ME\_FWP

19 ME\_FWP\_R

## Debug Connector



## Firmware SW



	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override

MESW1\_B  
ME\_FWP\_R  
ME\_FWP

AFTP6801 AFTE14P-GP  
AFTP6802 AFTE14P-GP  
AFTP6803 AFTE14P-GP

BOLT 15 32bit 0822



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Dubug connector**

Size  
A4

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

Sheet 68 of 106



www.teknisi-indonesia.com

(Blanking)

BOLT 15 32bit 0822



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

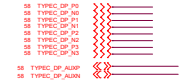
Sheet 69 of 105



From USB HOST



From DP Demux



From CCG4



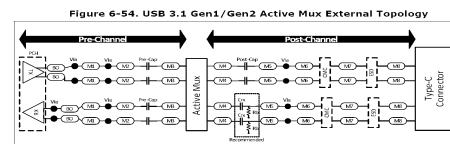
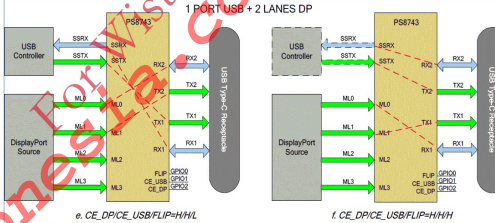
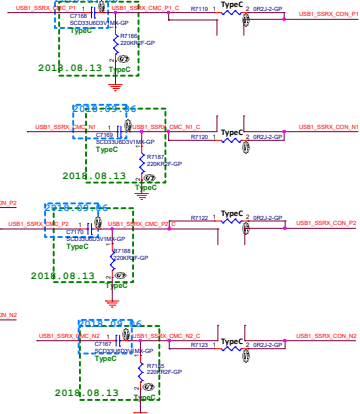
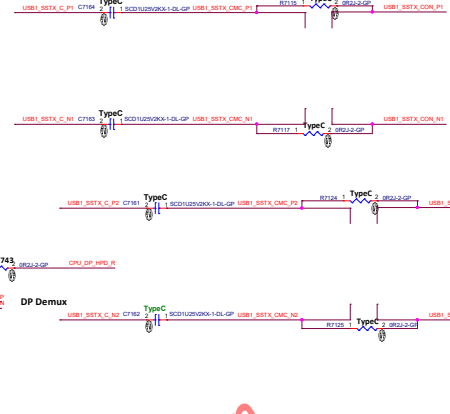
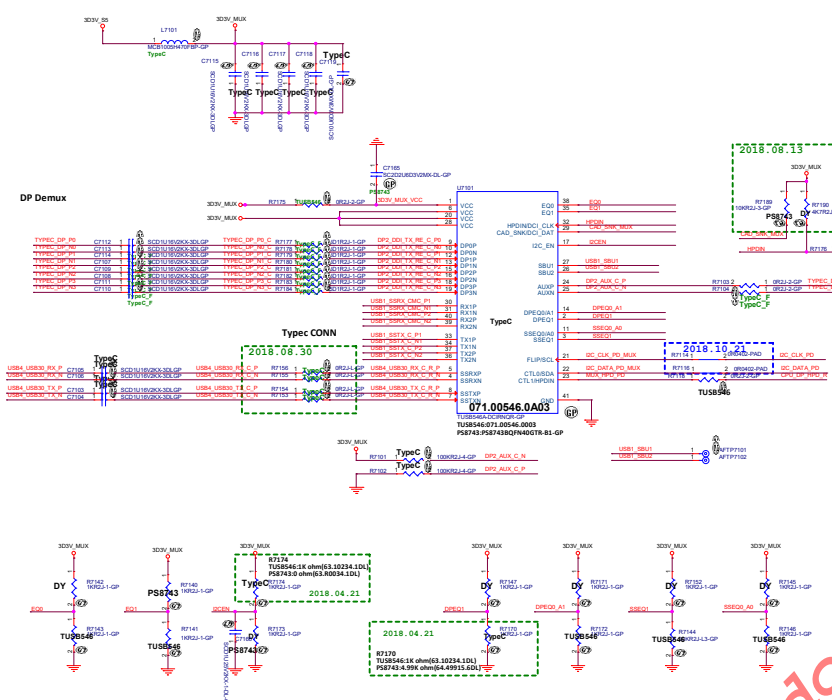
From CCG4 to MUX & DP Demux



To Type-C CONNECTOR



USB HOST

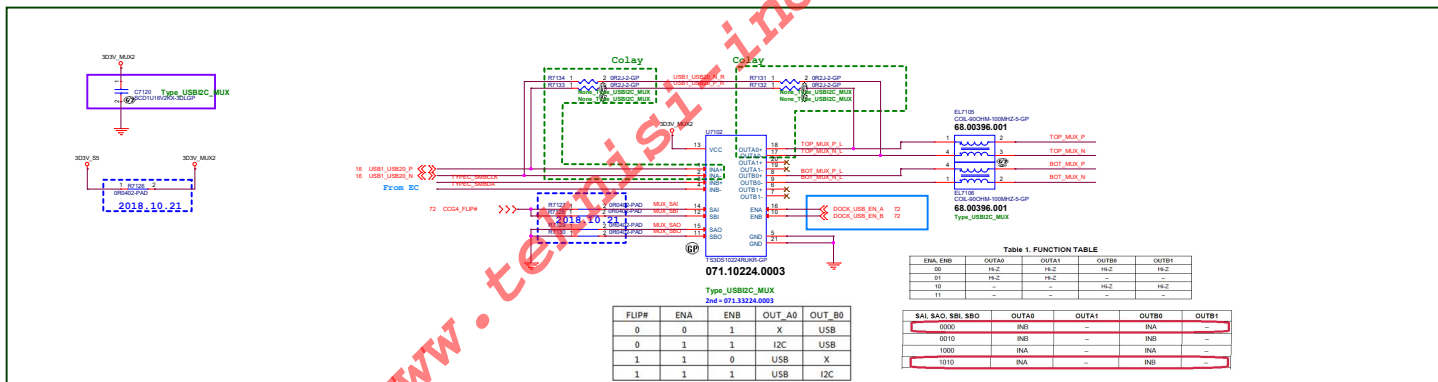
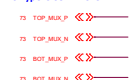


Channel	Parameter	Segment	Stackup	Via Count	Gen2	
					Length (mm)	Length (mils)
Pre-channel	Max Trace Length	B0	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M1	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M2-M3	M5	0	Note#1*	Note#1*
Post-channel	Max Trace Length	M4 + M5	M5	1	7.6	300
	Max Trace Length	M6-M7	M5	0	7.6	300
	Max Trace Length	M8	M5	1	10.2	400

From EC



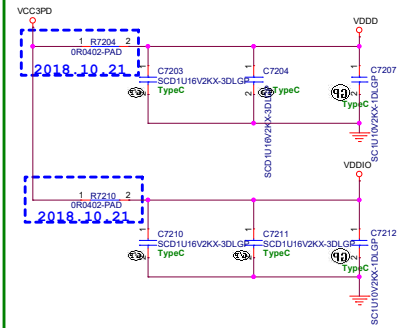
To Type-C CONNECTOR



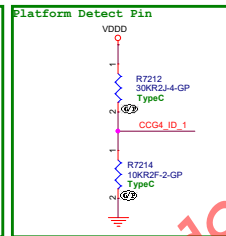
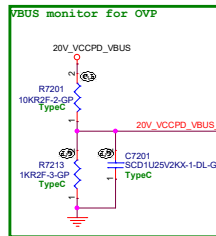
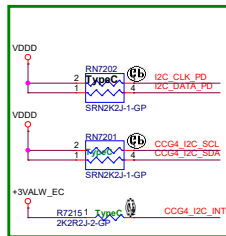
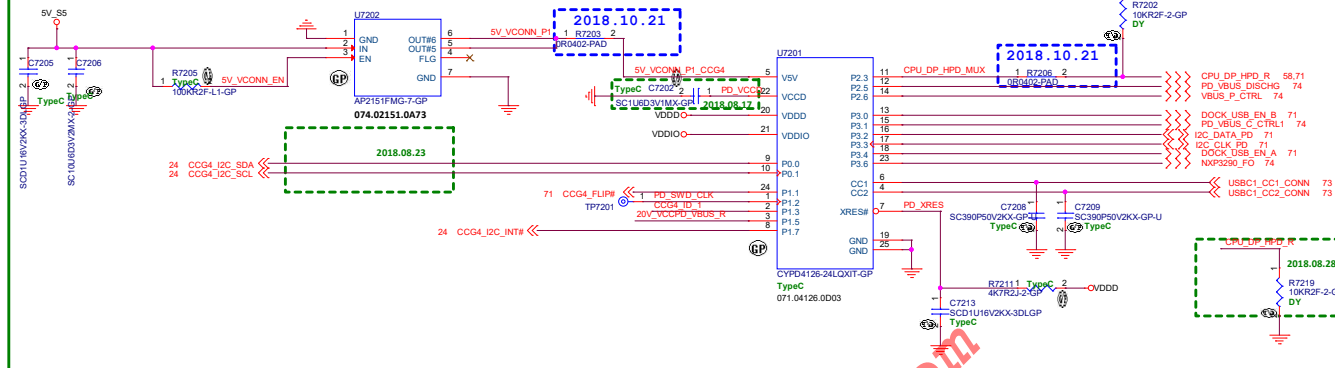
FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	00	00	00	00	00
01	01	01	01	01	01
10	10	10	10	10	10
11	11	11	11	11	11

## Power



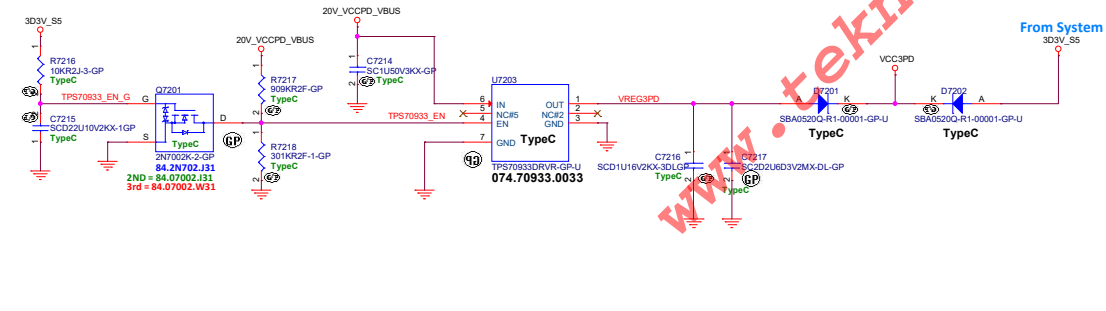
## TYPE C CONTROLLER



	CCG4 ID 1	R7212	R7214	計算値	理論値
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.12035.6DL (120K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

S.No	Project Name	ODM	CCG4 ID 1	Single/ Dual Port	Port 1 Configuration	Port 2 Configuration	Voltage level	Voltage value
1	Bolt (VHL) Data Only with PS8743B Max	Wistron	L0	Single	USB	N/A	1.0	0V
2	Bolt (VHL) Data Only with TUSB546 Max	Wistron	L1	Single	USB	N/A	1.1	3.3V/8
3	Bolt (VHL) Data Only with PS8743B Max	Wistron	L2	Single	USB	N/A	1.2	2 * 3.3V/8
4	Bolt (VHL) Data Only with TUSB546 Max	Wistron	L3	Single	USB	N/A	1.3	3 * 3.3V/8
5	Bolt (VHL) Full Feature with PS8743B Max	Wistron	L4	Single	USB+DP+ PD Charging	N/A	1.4	4 * 3.3V/8
6	Bolt (VHL) Full Feature with TUSB546 Max	Wistron	L5	Single	USB+DP+ PD Charging	N/A	1.5	5 * 3.3V/8
7	Bolt (VHL) Full Feature with PS8743B Max	Wistron	L6	Single	USB+DP+ PD Charging	N/A	1.6	6 * 3.3V/8
8	Bolt (VHL) Full Feature with TUSB546 Max	Wistron	L7	Single	USB+DP+ PD Charging	N/A	1.7	7 * 3.3V/8

## For Dead Battery modify



BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
		Title: <b>USB3.0 PORT</b>	
Size	Document Number	Rev	
Custom	<b>BOLT WHL</b>		<b>A00</b>
Date:	Thursday, December 27, 2018	Sheet	72 of 105



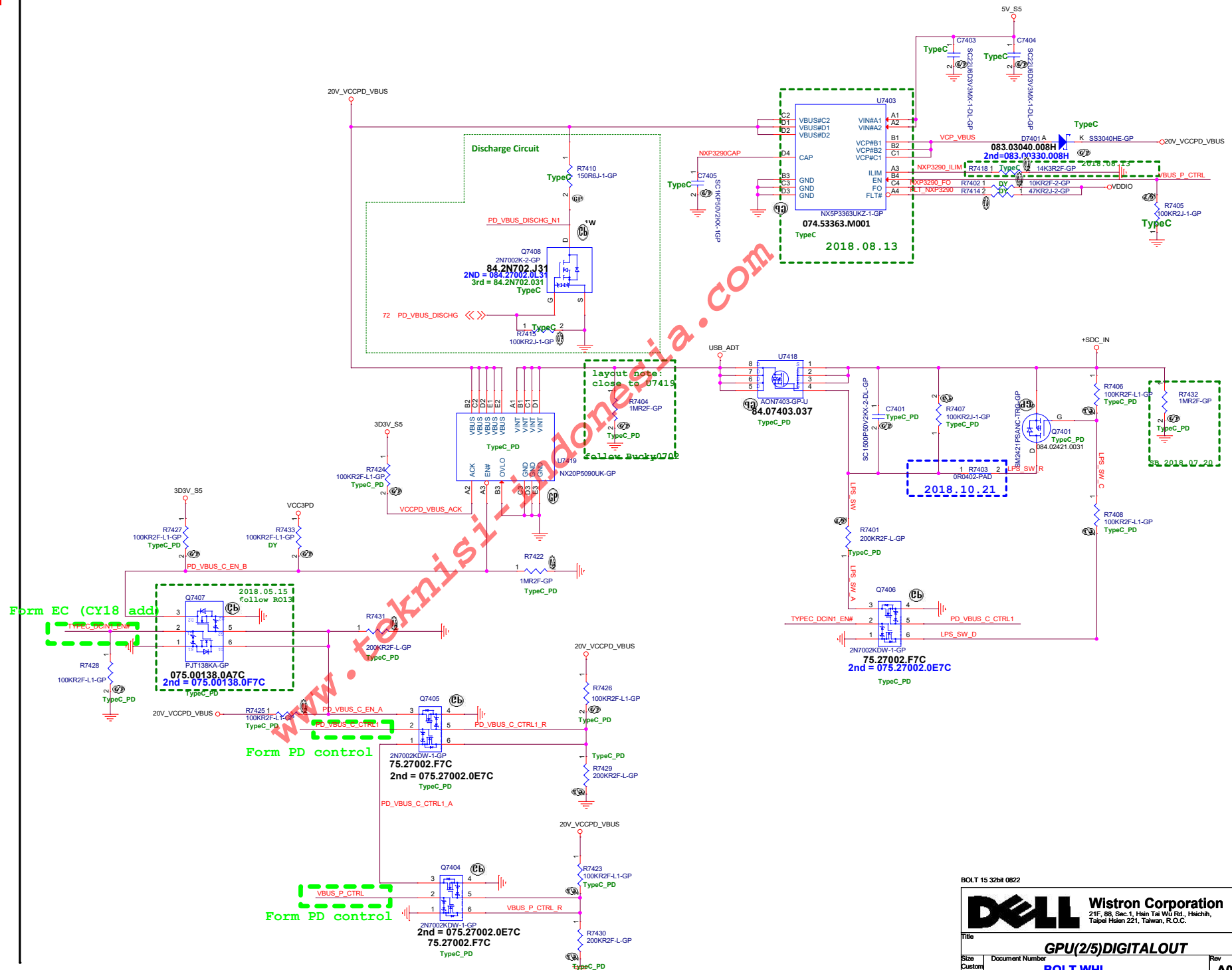
**Main FUNC = LPS**

```

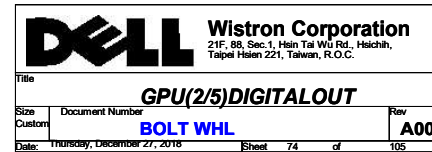
72 PD_VBUS_C_CTRL1 >>>_____
72,74 VBUS_P_CTRL >>>_____
24 TYPEC_DCIN1_EN# >>>_____
72 NXP3290_FO <<<_____
2,74 VBUS_P_CTRL >>>_____

```


4 VCCPD\_VBUS\_ACK >>



BOLT 15 32bit 0822



(Blanking)

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU(3/5)VRAM/I/F</b>			
Size	Document Number		Rev
A3	<b>BOLT WHL</b>		<b>A000</b>
Date:	Thursday, December 27, 2018	Sheet	75 of 106







1.35V +/- 3%  
4.88A

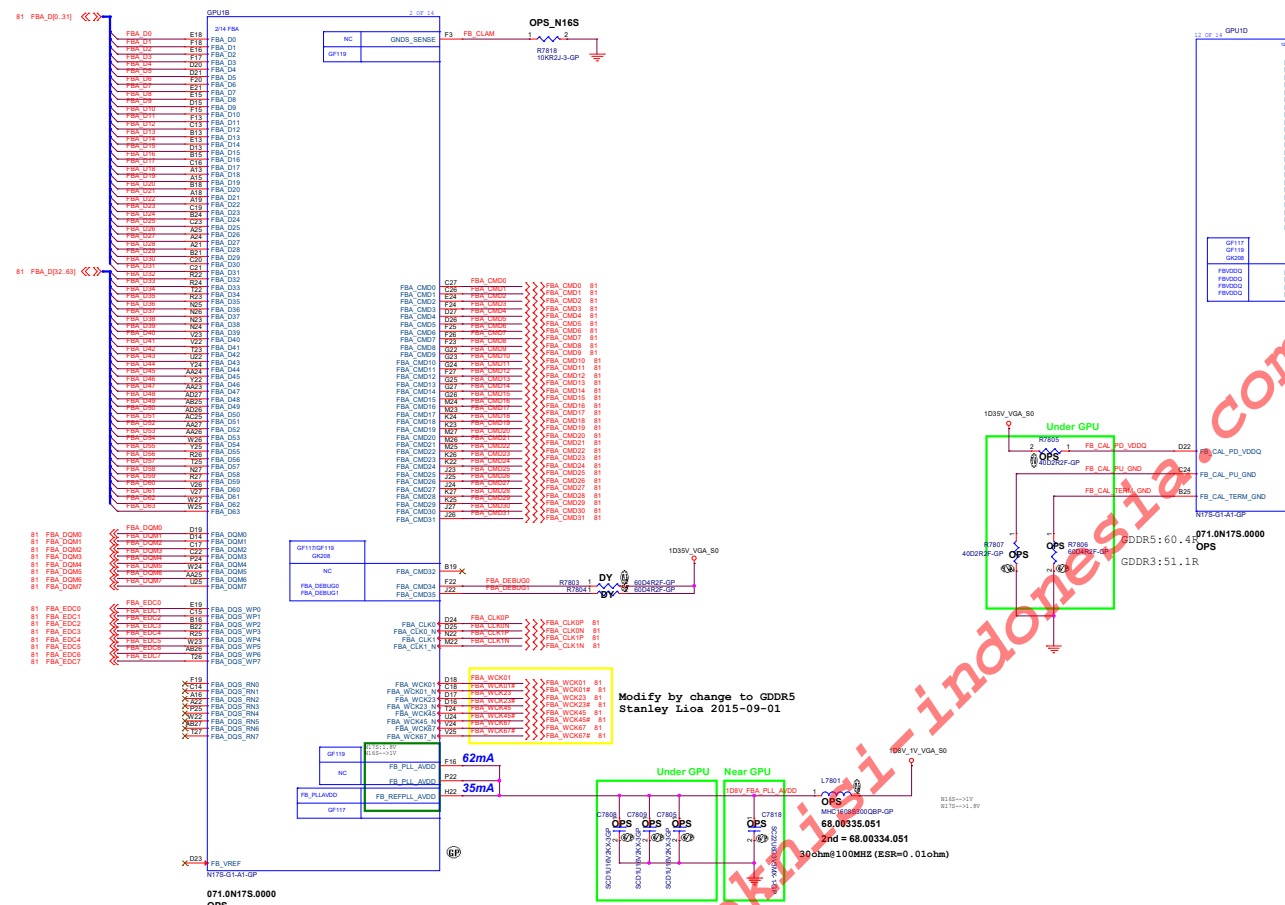
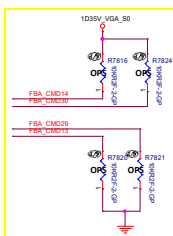


Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint	Population	Location	
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

Modify by change to GDDR5  
Stanley Lioa 2015-09-01

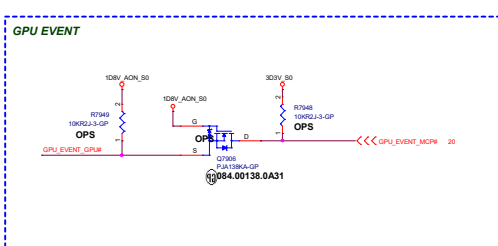


Note:  
Reference NV-DDR5 CRB and DOH70 by GDDR5

Table 3-37. GPCPLL\_AVDD0/1, LXS\_PLLVDD, and FB\_PLL\_DLL\_AVDD0/1 Power Rail Filter Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB3B-256	GPCPLL_AVDD0/1 + LXS_PLLVDD + FB_PLL_DLL_AVDD0/1	0.1 µF X7R	0402	5	Under GPU
		22 µF X5R	0805	1	Near GPU
Bead Type					
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU

ROHS IS 52M 0822



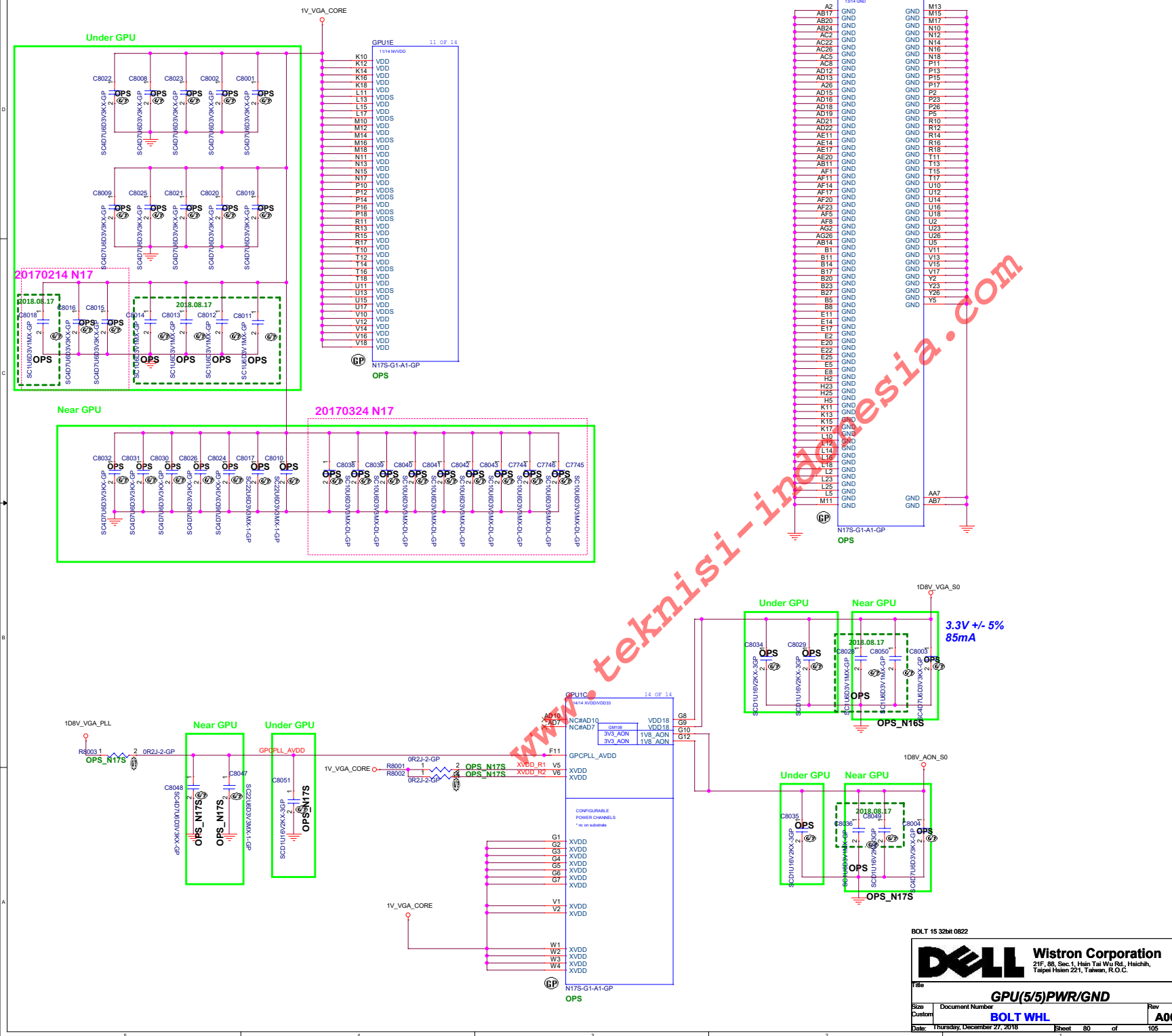
BOLT 15 5268 0622

**DELL** Wistron Corporation  
 21F, 8B, Sec 5, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsin 301, Taiwan, R.O.C.

File **GPU(4/5)GPIO/STRAP**

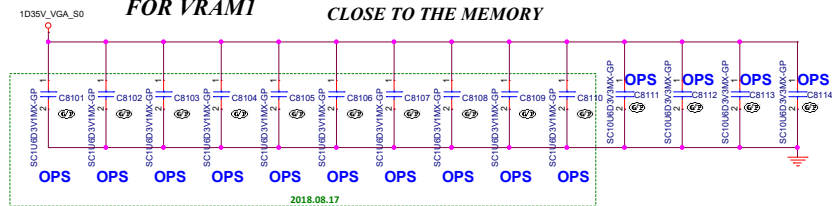
Size Custom	Document Number <b>BOLT WHL</b>	Rev A0
----------------	------------------------------------	-----------

## Main Func = dGPU



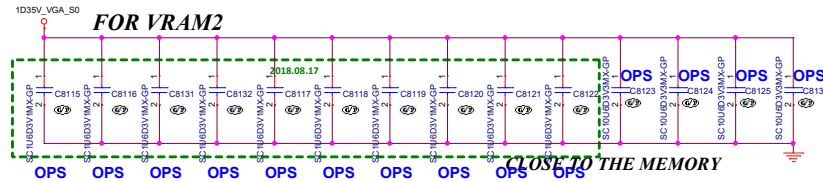
## FOR VRAM1

CLOSE TO THE MEMORY



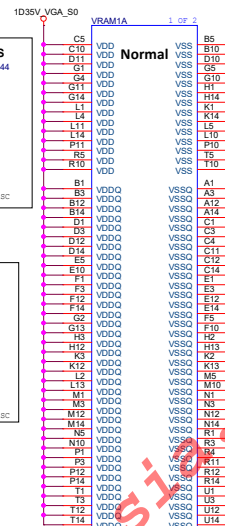
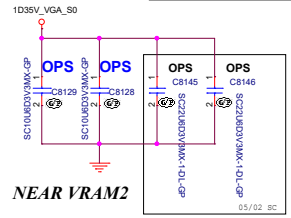
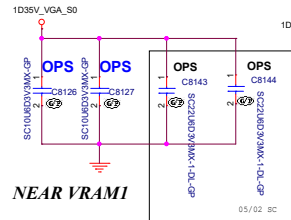
## FOR VRAM2

CLOSE TO THE MEMORY



## NEAR VRAM1

## NEAR VRAM2



Place close VDD ball

Place close VDD ball

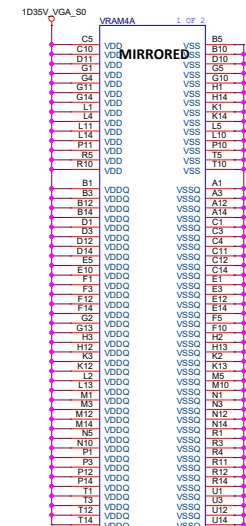
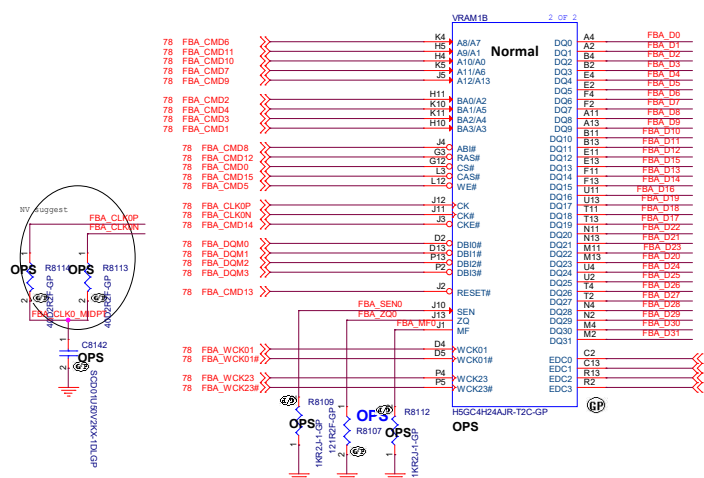


TABLE GDDR5 VIDEO MEMORY 072.05424.0A0U 072.44132.000U 072.04032.000N

	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BAGG-60-F-D
VRAM2			

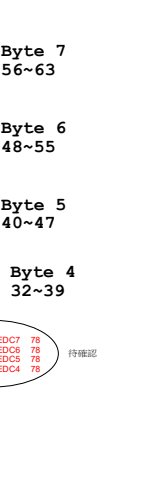
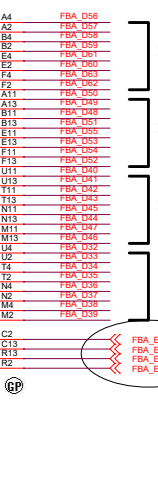
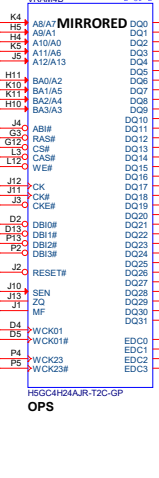
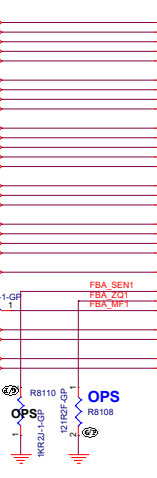
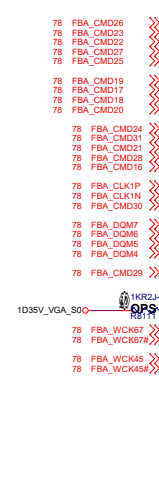
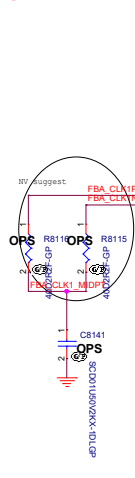


Byte 0

Byte 1

Byte 2

Byte 3



BOLT 15 32bit 0822

www.teknisi-indonesia.com

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822




**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>GPU-VRAM5,6 (3/4)</b>	
Size	Document Number	Rev		
A3	<b>BOLT WHL</b>	<b>A00</b>		
Date:	Thursday, December 27, 2018	Sheet	83	of 105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number		Rev
A3	BOLT WHL		A00
Date:	Thursday, December 27, 2018		Sheet 84 of 105





### PEX\_VDD

Chilisin. 2.5x2.0x1.2mm  
DCR: 34m~59m Ohm  
Ic: 3 A, Iest : 4 A

17S(Iccmax):0.2A  
17S(Icc):0.1A  
16S(Iccmax):2.1A  
16S(Iccmax):0.8A  
OPC>3A

V=0.6x((1+R1/R2)  
=0.6x((1+34/51)  
=1.009

[illegible]

		BOLT 15 32M 0822	
		<b>Wistron Corporation</b> 23F, 88, Sec. 1, Hsin-Yi Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
<b>DISCRETE VGA POWER</b>		Rev <b>A00</b>	
<b>BOLT WHL</b>		Sheet 86 of 106	
Date: Thursday, December 27, 2018		Sheet 86 of 106	

	<b>緯創資通</b> <b>Wistron Corporation</b> <small>21F, 88, Sec.1, Hsin-Tai Rd, Hsin-Tai, Hsinchu, Taiwan, R.O.C.</small>
<b>DISCRETE VGA POWER</b>	
Item: <b>BOLT WHL</b>	Rev: <b>A00</b>
Date: Thursday, October 27, 2016      Sheet: 86 of 106	

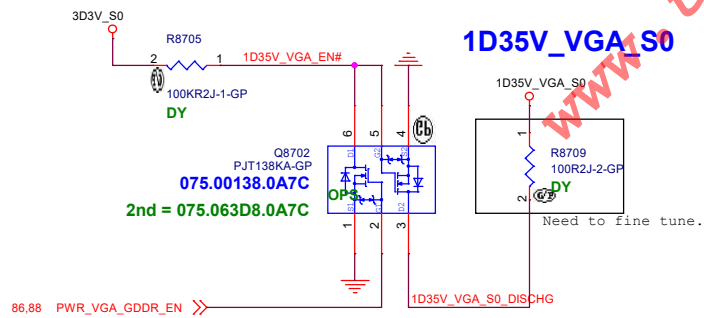
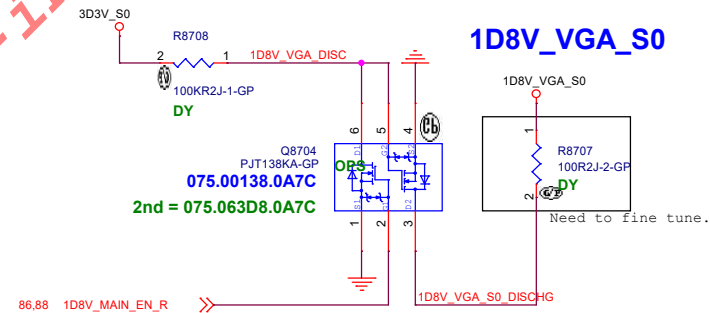
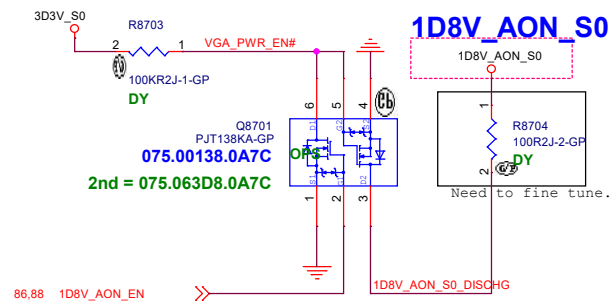
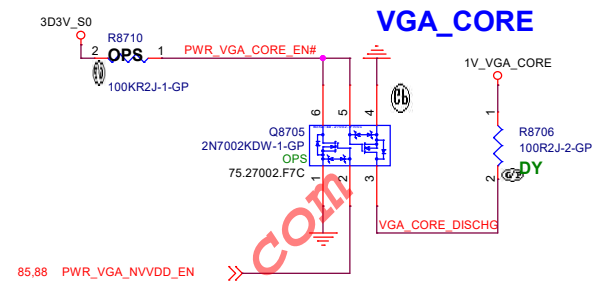
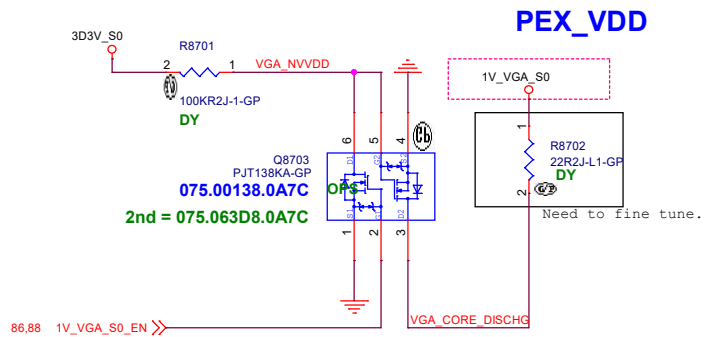
<b>DISCRETE VGA POWER</b>		Rev <b>A00</b>
Doc Customer	Document Number <b>BOLT WHL</b>	
Date:	Thursday, December 27, 2018	Sheet 85 of 100

Document released under the  
**BOLT WHL**

Date: **Thursday, December 27, 2018**      Sheet **86** of **106**

**A00**

Date: Thursday, December 27, 2018	Sheet 86 of 106
-----------------------------------	-----------------



BOLT 15 32bit 0822

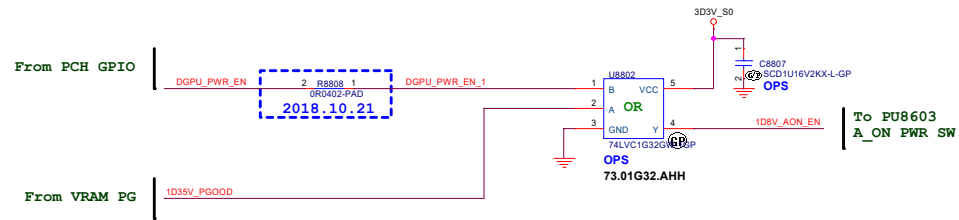


Title			Reserved	
Size	Document Number		Rev	
A3	BOLT WHL		A00	
Date:	Thursday, December 27, 2018		Sheet	87 of 105

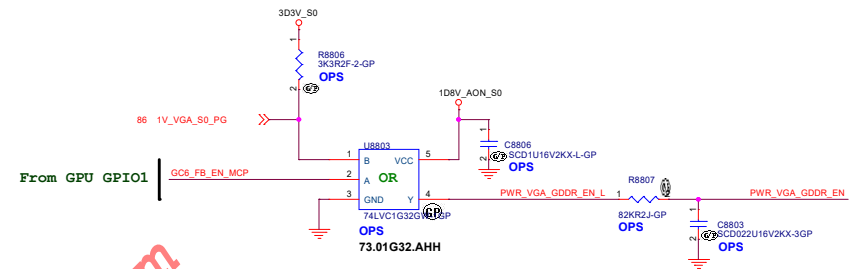
20 DGPU\_PWR\_EN >>>  
 85.86 1D35V\_PGOOD >>>  
 86.87 1D8V\_AON\_EN <<<  
 79 1D8V\_MAIN\_EN >>>  
 86.87 1D8V\_MAIN\_EN\_R >>>  
 85.87 PWR\_VGA\_NVVDD\_EN <<<

86.87 1V\_VGA\_S0\_EN <<<  
 20.79 GC6\_FB\_EN <<<  
 86.87 PWR\_VGA\_GDDR\_EN <<<

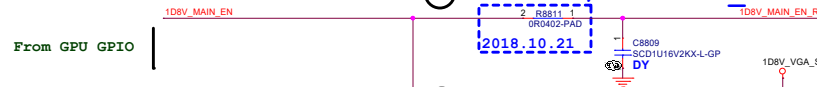
## ① Turn ON/OFF 1V8\_AON



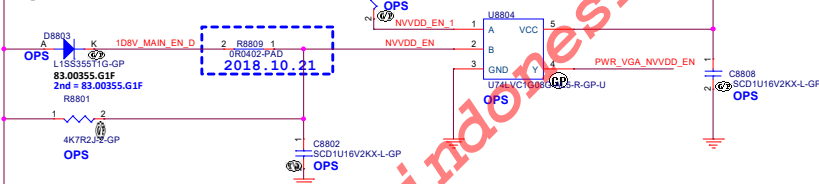
## ⑤ Turn ON/OFF FBVDD



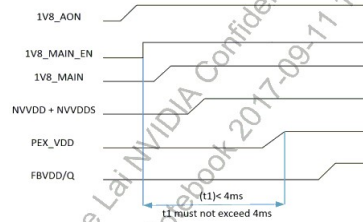
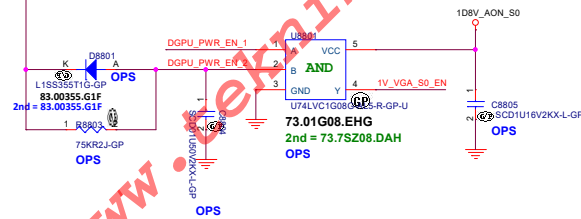
## ② Turn ON/OFF 1D8V\_MAIN



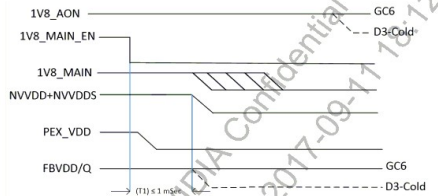
## ③ Turn ON/OFF NVVDD



## ④ Turn ON/OFF PEX\_VDD



### Power-Down Sequence

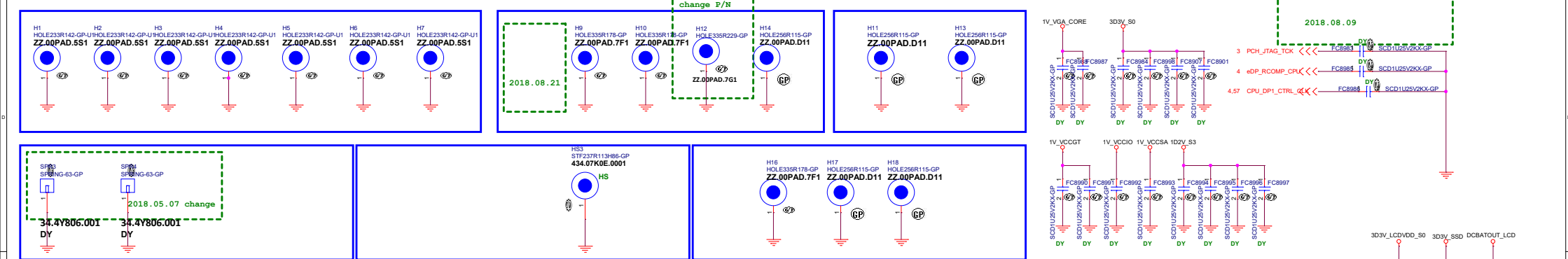


1V8\_AON  
 1V8\_MAIN\_EN  
 1V8\_MAIN  
 NVVDD + NVVDD5  
 PEX\_VDD  
 FBVDD/Q

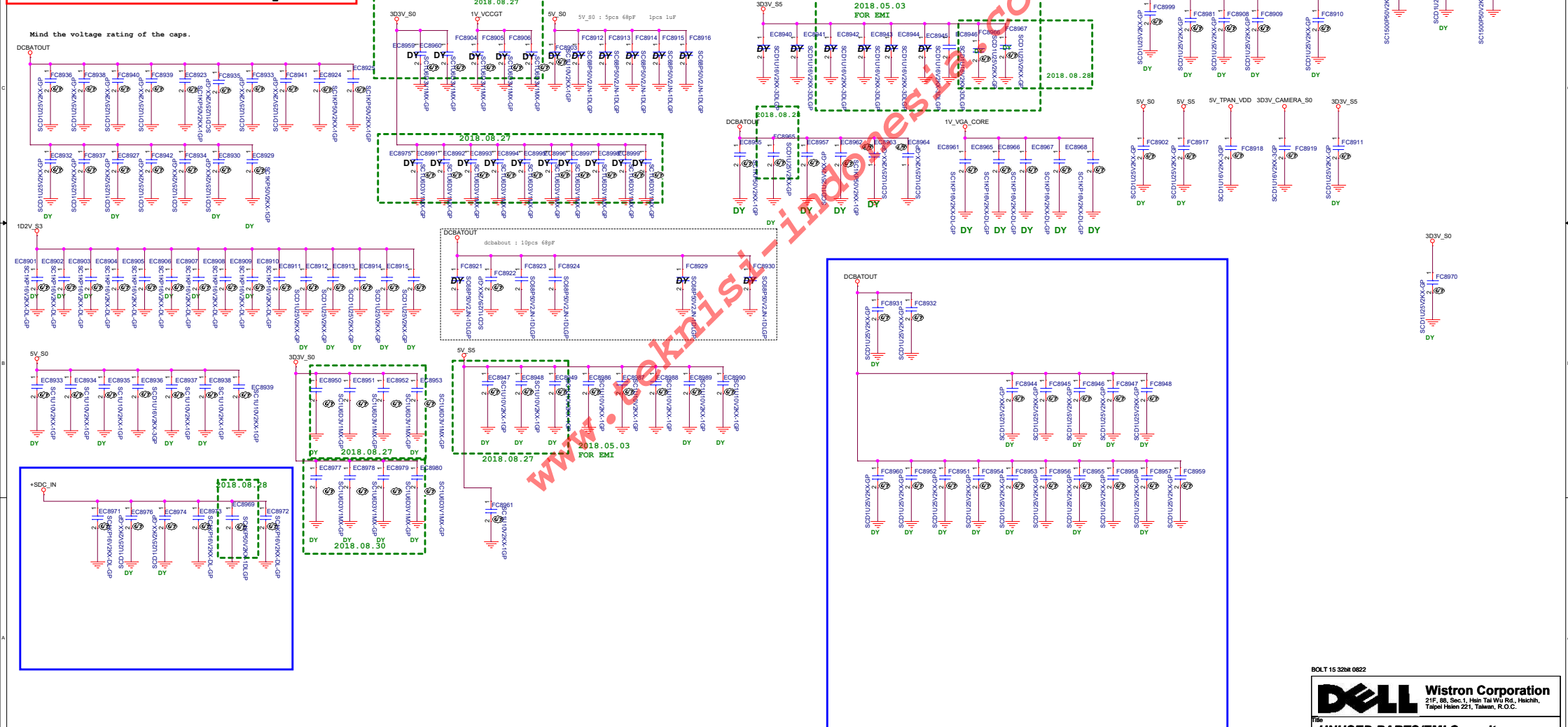
BOLT 15 32bit 0822

DELL Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hualien, Taipei Hualien 221, Taiwan, R.O.C.	
GPU SEQUENCE	
File	Rev
Size	Document Number
Custom	BOLT WHL
Date: Thursday, December 27, 2018	Sheet 88 of 105

# Main Func = UnusedParts



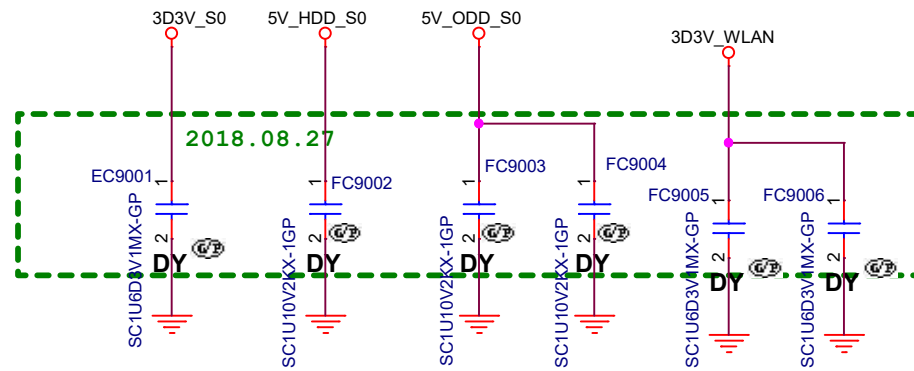
# Main Func = EMI & RF Capacitors



BOLT 15 32m 0822



File			Rev
UNUSED PARTS/EMI Capacitors			A00
Size	Document Number	BOLT WHL	
Date	Thursday, December 27, 2018	Sheet	89 of 105



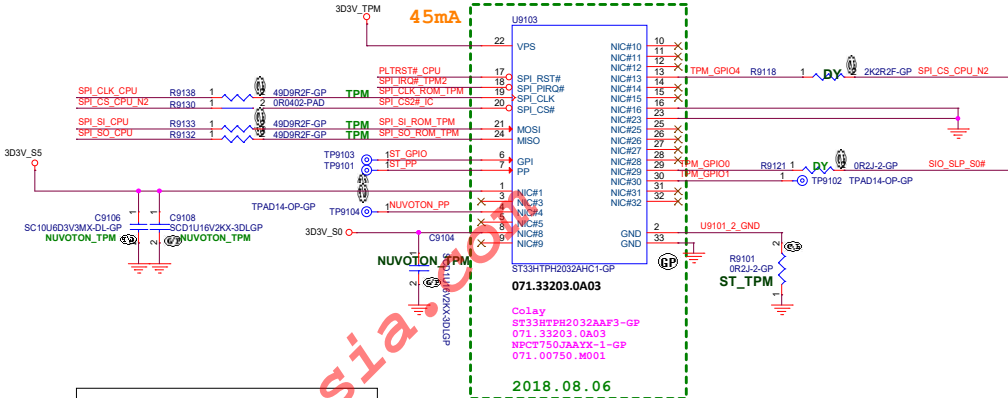
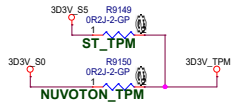
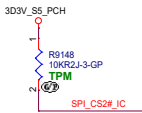
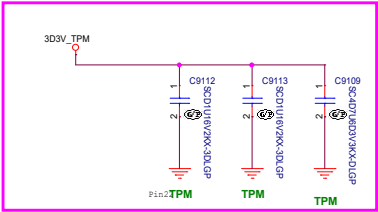
www.teknisi-indonesia.com

BOLT 15 32bit 0822

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018	Sheet 90	of	105


Main Func = TPM

- 18,25 SPI\_SO\_CPU <<< \_\_\_\_\_
- 18,25 SPI\_CLK\_CPU >>> \_\_\_\_\_
- 15,18,25 SPI\_SI\_CPU >>> \_\_\_\_\_
- 18 SPI\_CS\_CPU\_N2 <<< \_\_\_\_\_
- 17,26,31,61,62,63,76 PLTRST#\_CPU >>> \_\_\_\_\_
- 17,40 SIO\_SLP\_S0# >>> \_\_\_\_\_
- 20 PIRQ# <<< \_\_\_\_\_
- 18 TPM\_SPI\_IRQ# <<< \_\_\_\_\_



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File

**TPM2.0**

Size

Document Number

Rev

Custom

**BOLT WHL**

**A00**

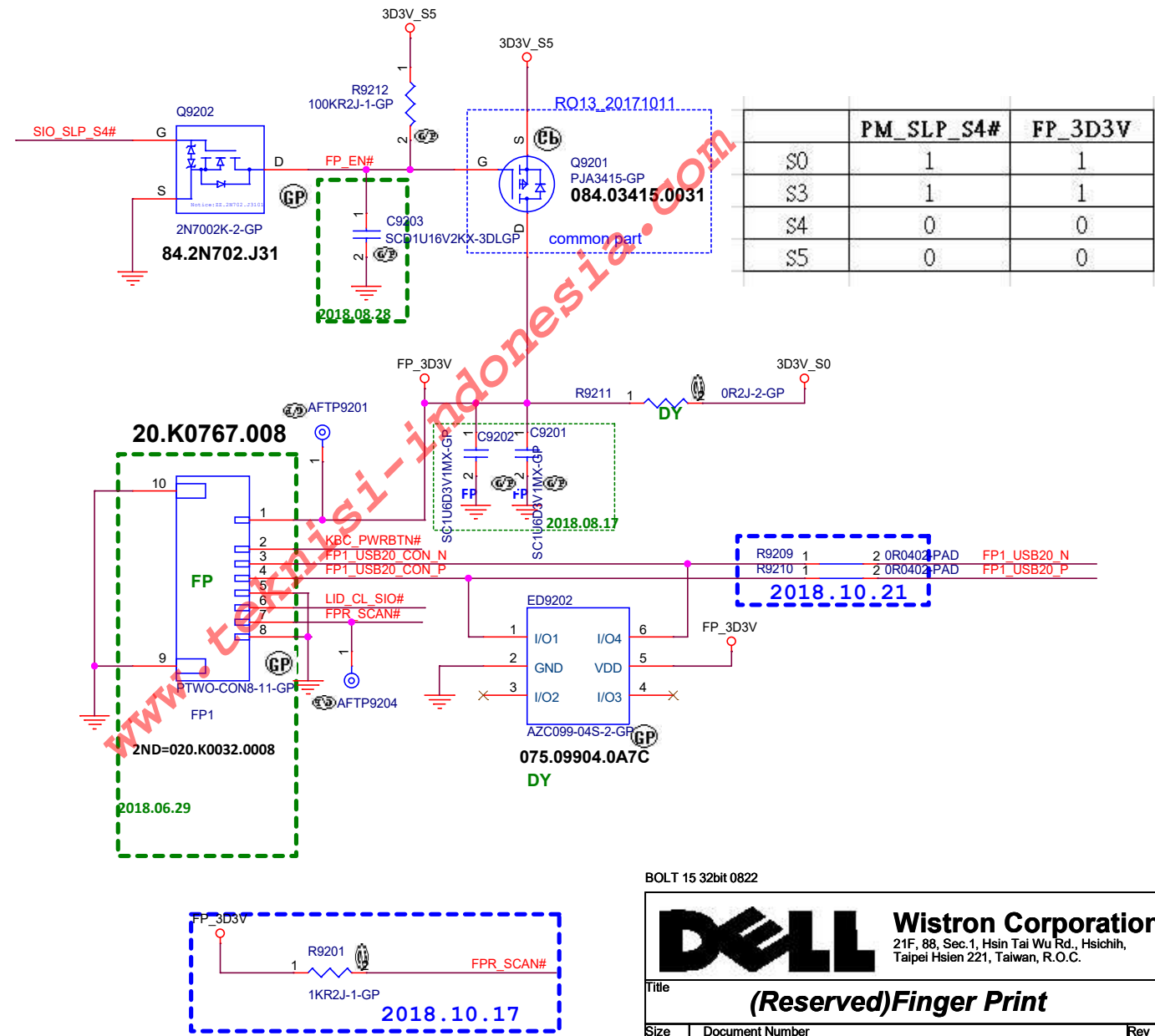
Date: Thursday, December 27, 2018

Sheet 91 of 105


Main FUNC = FPR

FBR(Botton side finger Print Sensor)

16 FP1\_USB20\_N >>>  
16 FP1\_USB20\_P >>>  
17,40,51 SIO\_SLP\_S4# >>>  
24,64 KBC\_PWRBTN# >>>  
24 FPR\_SCAN# >>>  
24,64 LID\_CL\_SIO# <<<



BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserved)Finger Print**

Size

Custom

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

Sheet 92 of 106



(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>(Reserved)</b>		
Size	Document Number				Rev
A3	<b>BOLT WHL</b>				<b>A00</b>
Date: Thursday, December 27, 2018		Sheet	93	of	105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>(Reserved)</b>		
Size	Document Number				Rev
A3	<b>BOLT WHL</b>				<b>A00</b>
Date: Thursday, December 27, 2018		Sheet	94	of	105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>(Reserved)</b>		
Size	Document Number				Rev
A3	<b>BOLT WHL</b>				<b>A00</b>
Date: Thursday, December 27, 2018		Sheet	95	of	105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			(Reserved)		
Size	Document Number				Rev
A4	BOLT WHL				A00
Date:	Thursday, December 27, 2018			Sheet 96 of	105

(Blanking)

www.teknisi-indonesia.com

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**LVDS\_Switch**

Size  
A4

Document Number

**BOLT WHL**

Rev

**A00**


Date: Thursday, December 27, 2018

Sheet 97 of 105

(Blanking)

www.teknisi-indonesia.com

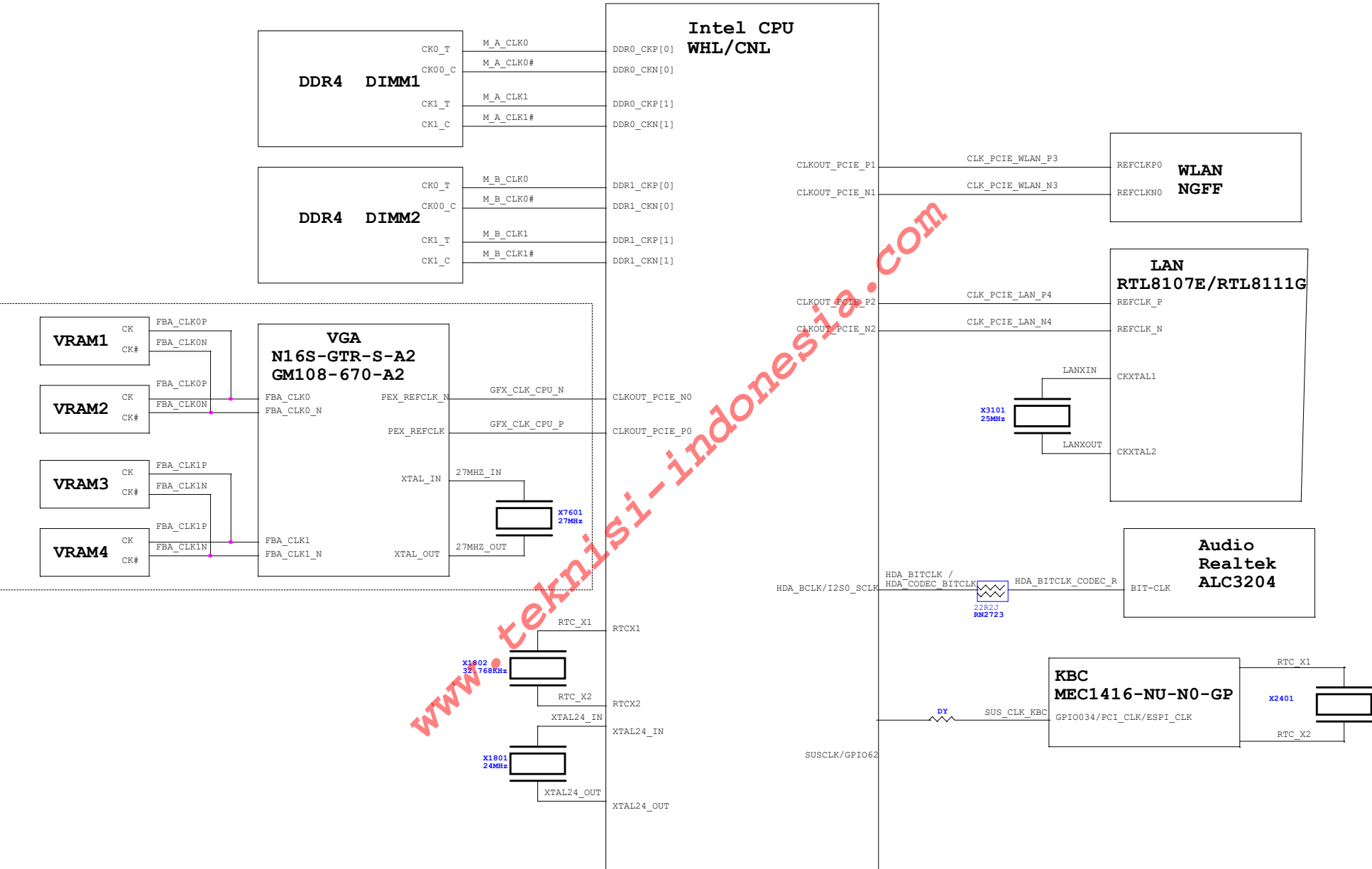
BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Firmware SW</b>			
Size	Document Number		Rev
A4	<b>BOLT WHL</b>		<b>A00</b>
Date:	Thursday, December 27, 2018		Sheet 98 of 105

(Blanking)

www.teknisi-indonesia.com

CLK Block Diagram



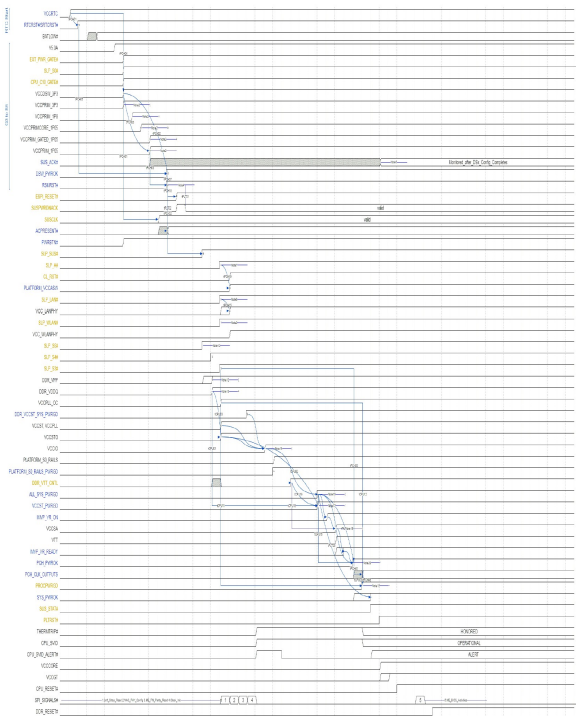


[illegible]

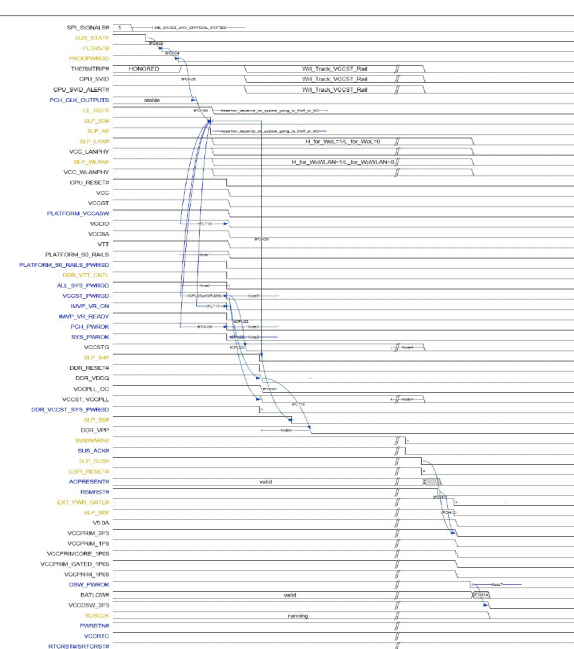
DELL

Sheet 101 of 105

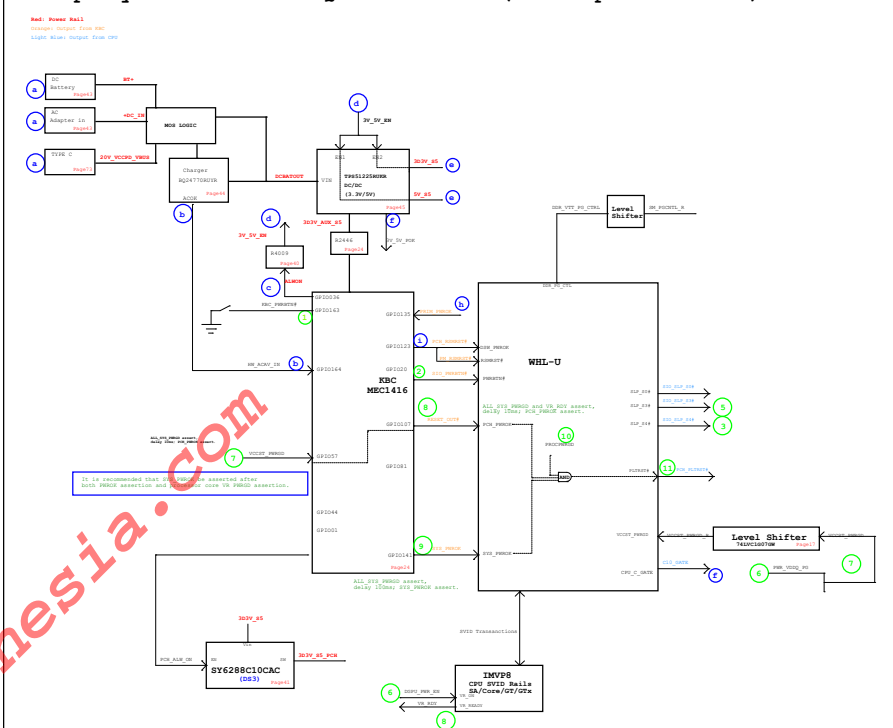
### CNL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



### WHL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



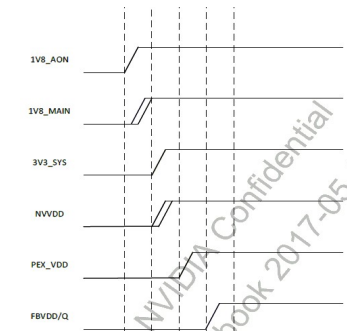
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



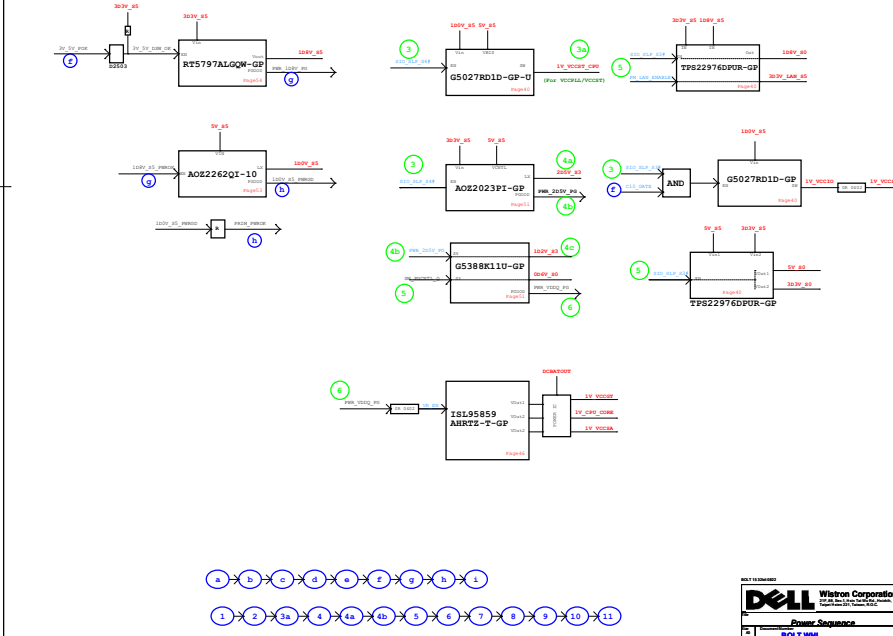
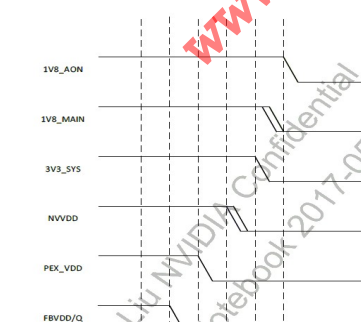
For DDR4 power sequence



## NVIDIA GPU Power up sequence

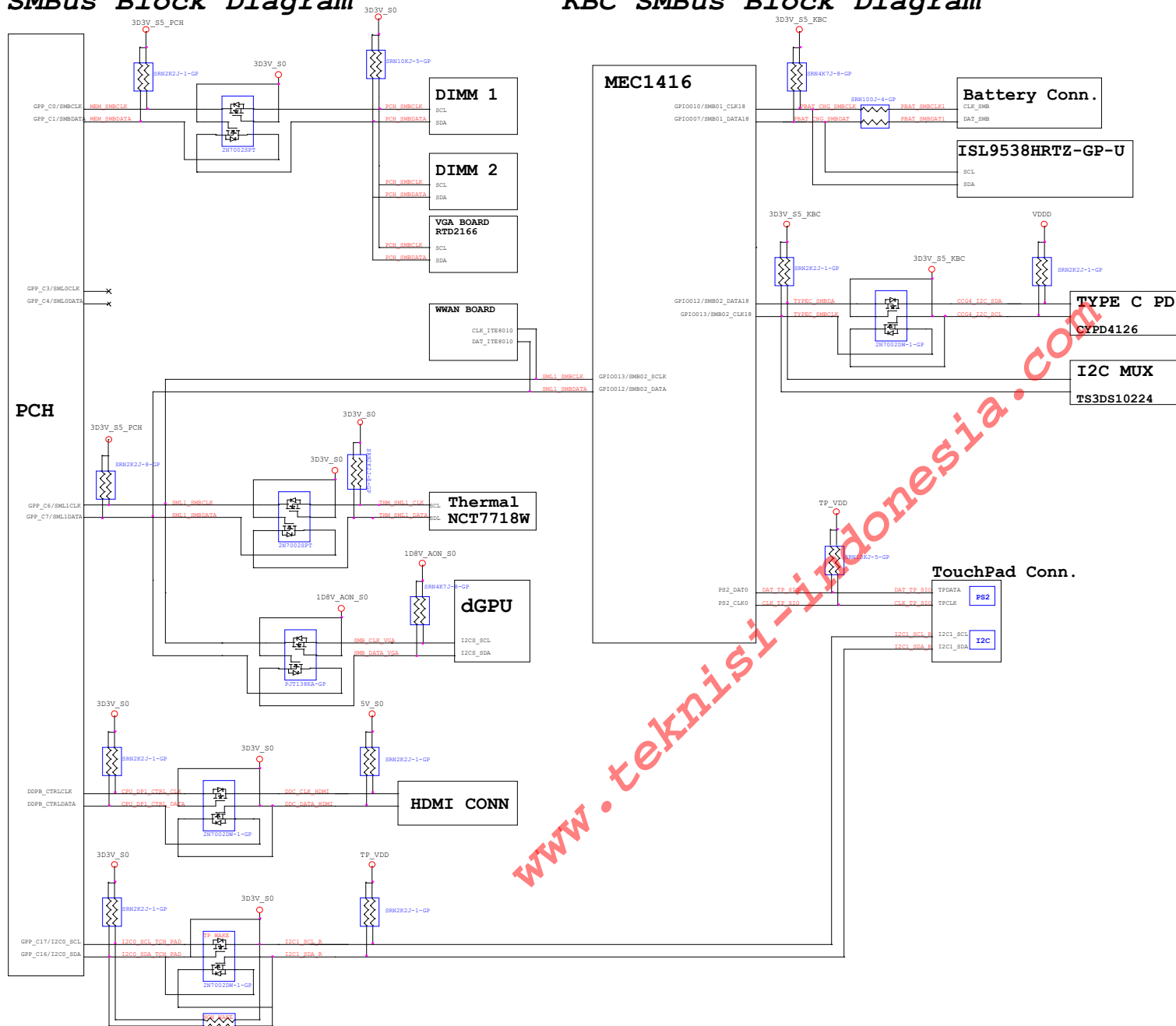


## NVIDIA GPU Power down sequence

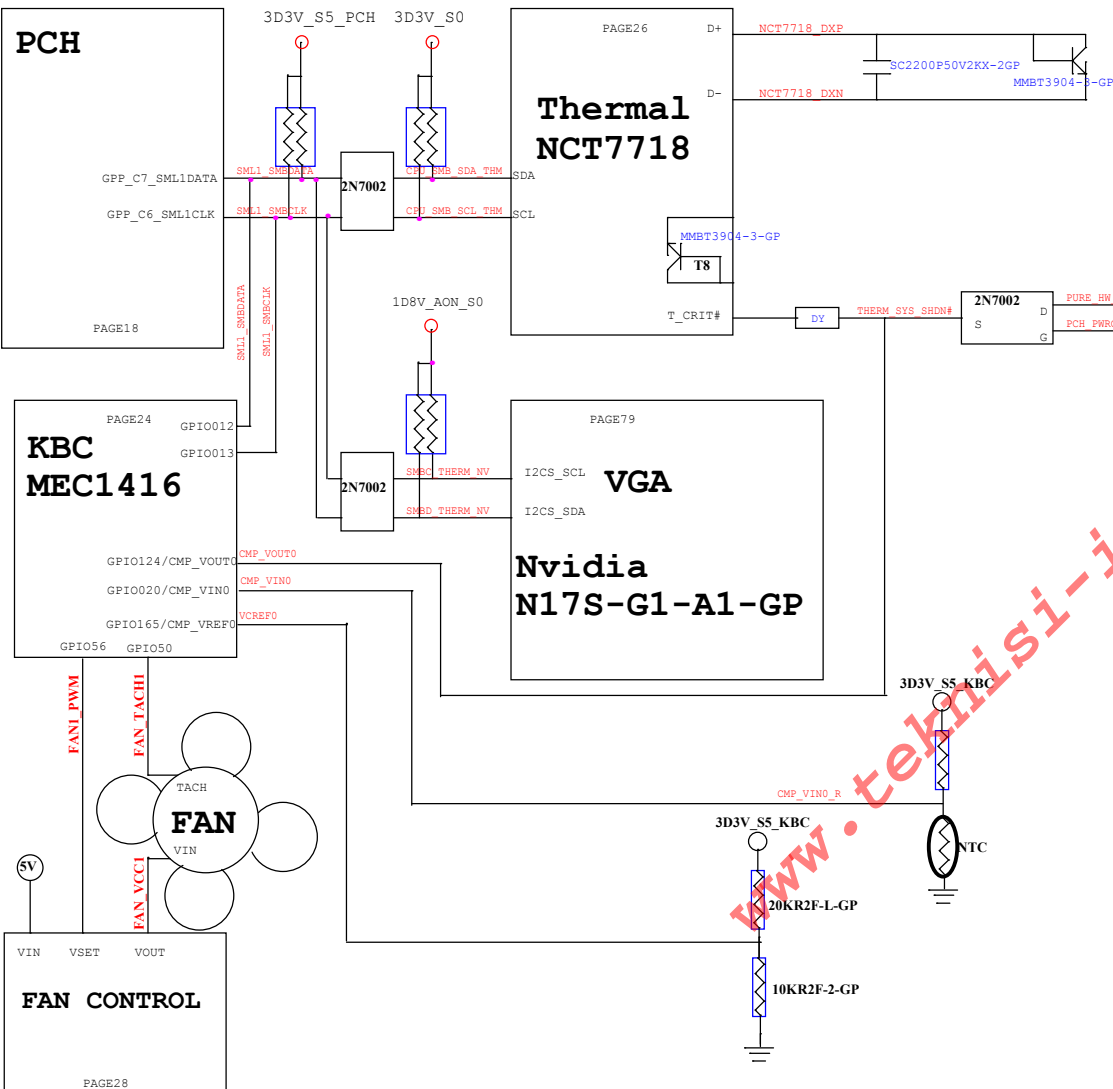




### KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram

